TECHNICAL REFERENCE NOTE

ARTESYN AIF06ZPFC SERIES

2400 W Full Brick PFC Converter

PRODUCT DESCRIPTION

Advanced Energy's Artesyn AIF06ZPFC series full-brick power factor correction module accepts a wide 85 to 264Vac input and presents a unity power factor. Rated at 2400 W, the module has a high conversion efficiency of 97.3% and provides a nominal non-isolated output voltage of 400Vdc. Featuring an industry-standard 2.4 x 4.6 in full-brick form factor and a height of only 0.55 in, they have a power density of 395 W/in^3.

AT A GLANCE

Total Power

1400 to 2400 W

Input Voltage

85 to 264 Vac

# of Outputs

Single

RoHS

SPECIAL FEATURES

- 2400 W continuous power high-line
- 1400 W continuous power low-line
- Ultra high efficiency: 97%
- 85 to 264 Vac input range
- Baseplate optimized for contact cooling or heatsink mounting
- Fixed switching frequency
- Pre-bias startup capability
- Programmable phase shift angle in parallel application
- High reliability
- RoHS 6 compliant
- UL94 V-0 materials
- PMBus™ communication
- Non-isolated PFC
- Feature rich control functions
- Standard full brick outline
- Parallel and current sharing version
- Internal inrush limit control (01 Version only)
- No external diodes required for two units sharing (external diodes required for >2)
- -40°C startup, -25°C operation
- Two-year warranty (consult factory for extended terms)

SAFETY

- CSA C22.2 No.62368-1
- CE EN62368-1
- UL 62368-1

TYPICAL APPLICATIONS

- Industrial
- Medical

MODEL NUMBERS

Standard	Input Voltage	Output Voltage	Minimum Load	Maximum Load	Efficiency
AIF06ZPFC-01***L	85-264Vac	400Vdc	0A	6A	97%
AIF06ZPFC-02***L	85-264Vac	400Vdc	0A	6A	97%

Note***:

AIF06ZPFC-01L	Single module operation and 2-module power sharing operation, Positive enable, RoHS-6, Threaded-inserts for mounting
AIF06ZPFC-01NL	Single module operation and 2-module power sharing operation, Negative enable, RoHS-6, Threaded-inserts for mounting
AIF06ZPFC-02L	3 to 6 modules power sharing operation, External diodes required, Positive enable, RoHS-6, Threaded-inserts for mounting
AIF06ZPFC-02NL	3 to 6 modules power sharing operation, External diodes required, Negative enable, RoHS-6, Threaded-inserts for mounting
AIF06ZPFC-01NTL	Single module operation or 2-module power sharing operation, Positive enable, RoHS-6, Non-Threaded-inserts for mounting
AIF06ZPFC-01NNTL	Single module operation or 2-module power sharing operation, Negative enable, RoHS-6, Non-Threaded-inserts for mounting
AIF06ZPFC-02NTL	3 to 6 modules power sharing operation, External diodes required, Positive enable, RoHS-6, Non-Threaded-inserts for mounting
AIF06ZPFC-02NNTL	3 to 6 modules power sharing operation, External diodes required, Negative enable, RoHS-6, Non-Threaded-inserts for mounting

Order Information

AIF	06	ZPFC	-	01	N	NT	L
①	②	③		④	⑤	⑥	⑦

①	Model series	Full brick size unit, AIF, full brick.
②	Output current	06: 6A rated output current
③	Output voltage	ZPFC: Power factor correction module, the output is 400Vdc
④	Model variant	01: The variant that can be stand-alone or 2 in parallel 02: External diodes required for more than 2 in parallel
⑤	Remote on/off logic	Blank is default and Positive enable. N: Negative enable
⑥	Structure	Blank is default with M3 thread. NT: Non-threaded-inserts for mounting
⑦	RoHS status	L: RoHS R6

Options

None

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Stress in excess of those listed in the "Absolute Maximum Ratings" may cause permanent damage to the power supply. These are stress ratings only and functional operation of the unit is not implied at these or any other conditions above those given in the operational sections of this TRN. Exposure to any absolute maximum rated condition for extended periods may adversely affect the power supply's reliability.

Table 1. Absolute Maximum Ratings

Parameter	Model	Symbol	Min	Typ	Max	Unit
Input Voltage Operating-Continuous Surge Voltage (1 sec)	All modules	$V_{IN,AC}$	85 -	- -	264 290	Vac Vac
Input Frequency	All modules		47	50/60	63	Hz
Maximum Output Power $85 \le V_{IN,AC} < 180$Vac $180 \le V_{IN,AC} < 200$Vac $200 \le V_{IN,AC} < 264$Vac	All modules	$P_{O,max}$	- - -	- - -	1400 2200 2400	W W W
Surge Load - Repetitive $85 \le V_{IN,AC} < 180$Vac $180 \le V_{IN,AC} < 200$Vac $200 \le V_{IN,AC} < 264$Vac	All modules	I_{O_surge}	- - -	- - -	4.5 8.0 9.0	A A A
Surge Load < 10ms $85 \le V_{IN,AC} < 180$Vac $180 \le V_{IN,AC} < 200$Vac $200 \le V_{IN,AC} < 264$Vac	All modules	I_{O_surge}	- - -	- - -	6.0 16.0 18.0	A A A
Isolation Voltage Input to Baseplate Output to Baseplate	All modules		- -	- -	4000 4000	Vdc Vdc
Input to Baseplate Capacitance	All modules		-	-	1300	pF
Operating Case Temperature	All modules	$T_{\_BP}$	-25	-	100	°C
Startup Case Temperature	All modules	$T_{\_BP}$	-40	-	100	°C
Storage Temperature	All modules	T_{STG}	-40	-	110	°C
Humidity (non-condensing) Operating Storage	All modules All modules		- -	- -	95 95	% %
MTBF Telcordia Issue 4, Method 1 Case1	All modules		1.0	-	-	M Hours
PMBus Clock Frequency	All modules	f	100	-	400	KHz

Note - Unless otherwise indicated, specifications applied over all operating input voltage and temperature conditions. Standard test condition on a single unit. See appendix A for test conditions and setup.

Note of caution

Please note that AIF06ZPFC is a non-isolated product between input and output terminals. Only the baseplate and mounting inserts can be considered as isolated from input and output. Please be cautioned that high voltage differential scope probe (500V or 1KV) or isolated oscilloscope should be used for any waveform monitoring or measurement due to safety consideration. Failure to observe this instruction can cause either incorrect measurements, or as a worst case, irreparable damage.

ELECTRICAL SPECIFICATIONS

Input Specifications

Table 2. Input Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Operating Input Voltage, AC	All	$V_{IN,AC}$	85	-	264	Vac
Input AC Frequency	All	f_{IN}	47	50/60	67	Hz
Maximum Input Current ($I_O = I_{O,max}$)	$V_{IN,AC}$ = 115Vac	$I_{IN,max}$	-	-	13.5	A
No Load Input Current (V_O Enable I_O = 0A)	All	I_{IN,no_load}	-	-	0.5	A
No Load Input Power (V_O Enable I_O = 0A)	All	P_{IN,no_load}	-	3	5	W
Harmonic Line Currents	All	THD	IEC 61000-3-2 for 1 module IEC 61000-3-12 for 2 or more modules in paralleled @ full load			
Power Factor	P_O > 700W P_O > 1400W	PF	0.96 0.98	0.97 0.99		
Startup Surge Current (Inrush)[2]	All	$I_{IN,surge}$	-	-	40	A
Input AC Low Line Start-up Voltage	$I_O = I_{O,max}$	$V_{IN,AC}$	81.5	-	84.5	Vac
Input AC Undervoltage Lockout Voltage	$I_O = I_{O,max}$	$V_{IN,AC}$	70.0	-	75.0	Vac
Efficiency	$V_{IN,AC}$ = 115Vac (1400W) $V_{IN,AC}$ = 230Vac (1400W) $V_{IN,AC}$ = 230Vac (2400W)	η	94.5 96.0 96.5	95.2 96.8 97.2	- - -	% % %
Turn On Delay[1]	$I_O = I_{O,max}$	T_{on_delay}	-	-	2	Sec
PF ENABLE - Module Enable Negative Enable	Module enabled	V_{PF_L}	0	-	0.8	V
	Module disabled	V_{PF_H}	2.2	-	3.3	V
PF ENABLE - Module Enable Positive Enable	Module enabled	V_{PF_H}	2.2	-	3.3	V
	Module disabled	V_{PF_L}	0	-	0.8	V
PF ENABLE Current Source	All	I_{PF}	-	-	300	uA

Note 1 - The 2 seconds max turn on delay time is for 01 version only.
Note 2 - The inrush current rating is for 01 version only.

ELECTRICAL SPECIFICATIONS

Output Specifications

Table 3. Output Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Factory Set Voltage	I_O = 3A	$V_{O,factory}$	397	400	403	Vdc
Maximum Output Power	85 ≤ $V_{IN,AC}$ < 180Vac 180 ≤ $V_{IN,AC}$ < 200Vac 200 ≤ $V_{IN,AC}$ < 264Vac	$P_{O,max}$	- - -	- - -	1400 2200 2400	W W W
V_O Load Capacitance[1]	All	-	680	-	2000	uF
Total Regulation	Inclusive of set-point, line, load temperature change, warm-up drift	±%V_O	-	-	2	%
Output Voltage Adjust Range	All	V_O	330	-	400	Vdc
Output Voltage Ripple, pk-pk	Measure with a 2000uF bulk capacitor to 20MHz bandwidth $V_{IN,AC}$ = 115Vac, I_O = 3.5A $V_{IN,AC}$ = 230Vac, I_O = 6 A	$V_{O,ripple}$	- -	- -	28 30	V_{PK-PK} V_{PK-PK}
Output Current, peak	All	$I_{O,peak}$	0	-	6	A
Dynamic Response Peak Deviation	0 - 25% load change	±%V_O	-	12.5	-	%
Output Current, continous	All	I_O	0	-	6	A
Over Voltage Protection	All	V_O	445	450	455	Vdc
Over Temperature Protection	All	T	103	108	113	°C
Number of Parallel Units[2]	"C SHARE" connected		-	-	6	
V_O Current Share Accuracy	"C SHARE" connected		-	0.2	0.6	A/unit
CLK OUT- Clock Output	CLK IN open	$V_{CLK\ OUT}$	-	3.3	-	
	Clock frequency	f	272	280	288	KHz
CLK IN - Clock Input	All	$V_{CLK\ IN\_H}$	2.4	-	3.6	V_{PK-PK}
		$V_{CLK\ IN\_L}$	0	-	0.55	V_{PK-PK}
		f	266	280	294	KHz
PFW ADJ - Power Fail Warning Adjust[3]	0 to 2.95Vdc 3.20Vdc 3.40Vdc	V_{PFW}	302 305 325	307 320 340	312 335 355	Vdc Vdc Vdc
PFW ADJ Current Source		I_{PFW}	-	1	-	mA
PFW - Power Fail Warning	Input power OK	V_{PFW_H}	10.8	12.0	13.2	V
	Input power Fail	V_{PFW_L}	0	0.2	0.4	V
	PFW short to S GND	I_{PFW}	-	2.64	-	mA

Note 1 - 680uF not for full load.
Note 2 - Qualified with 3 modules only but it's capable for 6 modules maximum. AIF06ZPFC-01L supports 2 paralleled modules only.
Note 3 - Fault condition will override voltage setting condition. Detail please refer to the protection section.

ELECTRICAL SPECIFICATIONS

Output Specifications

Table 3. Output Specifications Con't

Parameter	Condition	Symbol	Min	Typ	Max	Unit
LD ENABLE - Load Enable[4]	Load enabled	V_{LD_H}	10.8	12	13.2	V
	Load disabled	V_{LD_L}	0	0.2	0.4	V
	LD ENABLE short to S GND	I_{LD}	-	2.64	-	mA
	Output Voltage Fail	$V_{O\_LD\_L}$	287	292	297	Vdc
PV AUX[5]	$I_{PV\ AUX}$ = 0A $I_{PV\ AUX}$ = 20mA	V_{PV}	10.8 10.8	12.0 12.0	13.2 13.2	V V
C Mon	Iout=6A		1.7	1.8	1.9	V
Temperature Tolerance to the Center of Base - plate		$\pm T_{mon}$	-	-	5	^{O}C

Note 4 - The output load will be controlled by LD Enable. The module will be forced into the initial start up state after LD enable go to low. Detail please refer to the Power and Control pin Description's LD section. Some fault conditions will override the $V_{O\_LD\_L}$ voltage level. Detail please refer to the protection section

Note 5 - PV AUX can be used at primary side only.

WARNING - LD ENABLE must be used to start the unit, otherwise the inrush resistor inside the module will be damaged or overstressed.

ELECTRICAL SPECIFICATIONS

AIF06ZPFC-01L Performance Curves

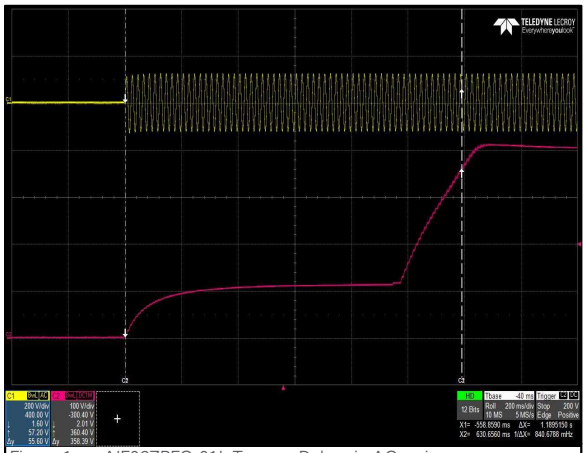


Figure 1: AIF06ZPFC-01L Turn-on Delay via AC mains
Vin = 85Vac Load: Io = 0A Co = 2000uF
Ch 1: Vin Ch 2: Vo

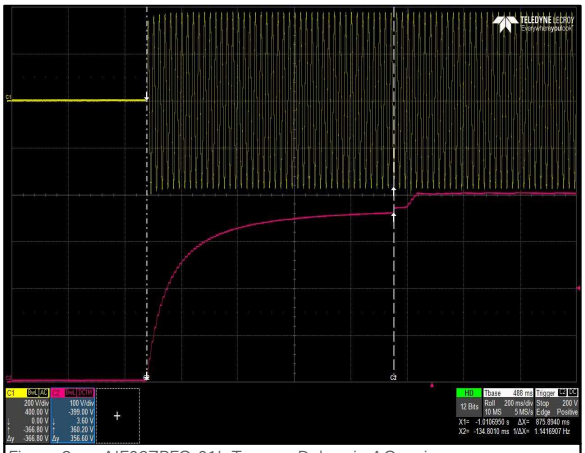


Figure 2: AIF06ZPFC-01L Turn-on Delay via AC mains
Vin = 264Vac Load: Io = 0A Co = 2000uF
Ch 1: Vin Ch 2: Vo

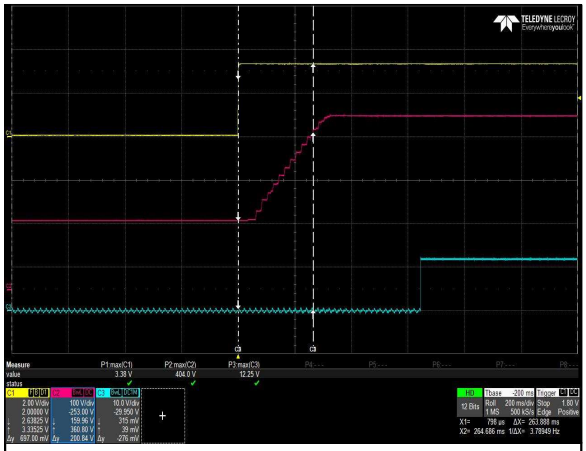


Figure 3: AIF06ZPFC-01L Turn-on delay via PF ENABLE
Vin = 115Vac Load: Io = 0A Co = 2000uF
Ch 1: PF ENABLE Ch 2: Vo Ch 3: LD ENABLE

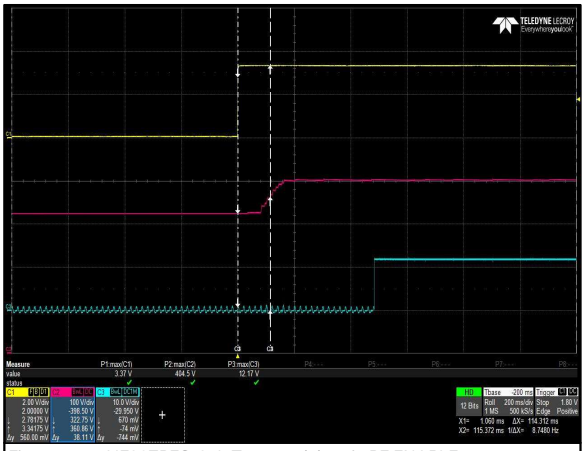


Figure 4: AIF06ZPFC-01L Turn-on delay via PF ENABLE
Vin = 230Vac Load: Io = 0A Co = 2000uF
Ch 1: PF ENABLE Ch 2: Vo Ch 3: LD ENABLE

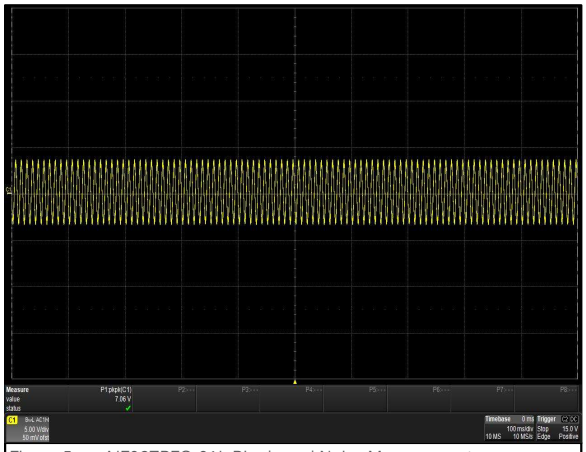


Figure 5: AIF06ZPFC-01L Ripple and Noise Measurement
Vin = 115Vac Load: Io = 3.5A Co = 2000uF
Ch 1: Vo

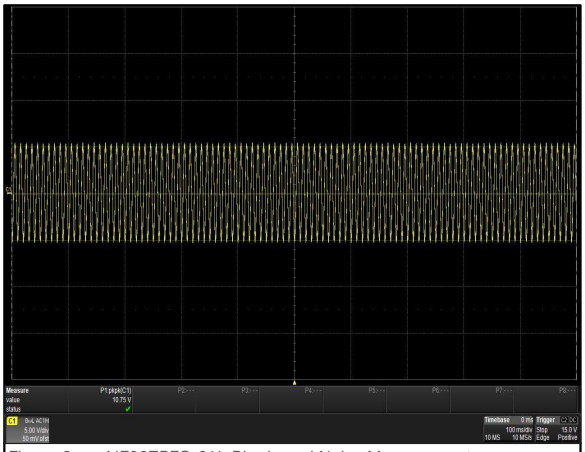


Figure 6: AIF06ZPFC-01L Ripple and Noise Measurement
Vin = 115Vac Load: Io = 6A Co = 2000uF
Ch 1: Vo

ELECTRICAL SPECIFICATIONS

AIF06ZPFC-01L Performance Curves

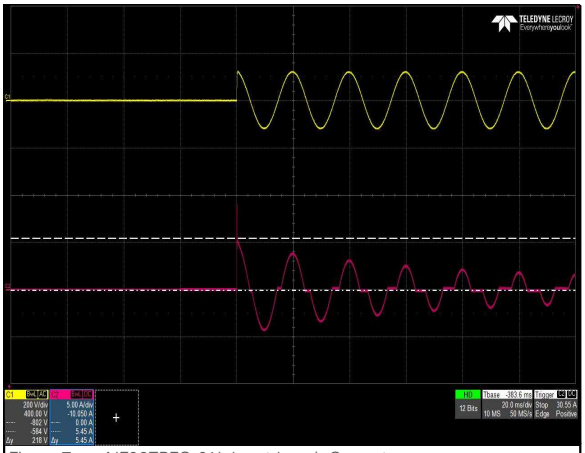


Figure 7: AIF06ZPFC-01L Input Inrush Current
Vin = 85Vac Load: Io = 0A Co = 2000uF
Ch 1: Vin Ch 2: Iin

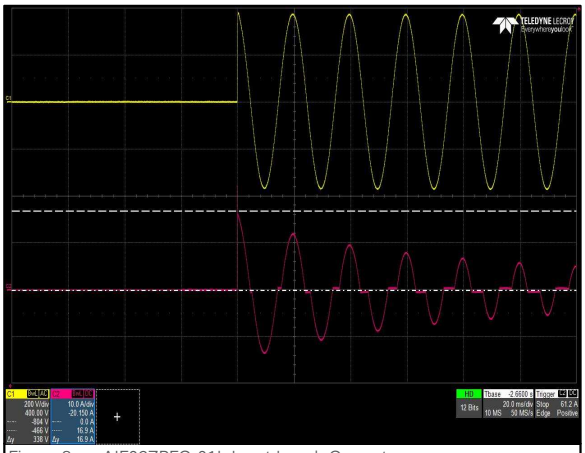


Figure 8: AIF06ZPFC-01L Input Inrush Current
Vin = 264Vac Load: Io = 0A Co = 2000uF
Ch 1: Vin Ch 2: Iin

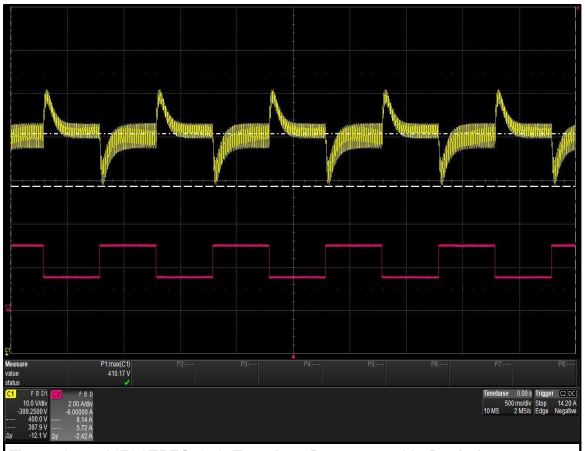


Figure 9: AIF06ZPFC-01L Transient Response - Vo Deviation
25% to 50% load change 1A/uS slew rate Co = 2000uF
Ch 1: Vo Ch 2: Io

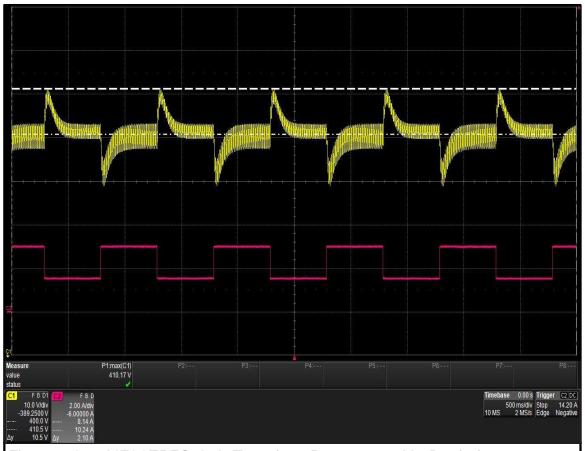


Figure 10: AIF06ZPFC-01L Transient Response - Vo Deviation
50% to 25% load change 1A/uS slew rate Co = 2000uF
Ch 1: Vo Ch 2: Io

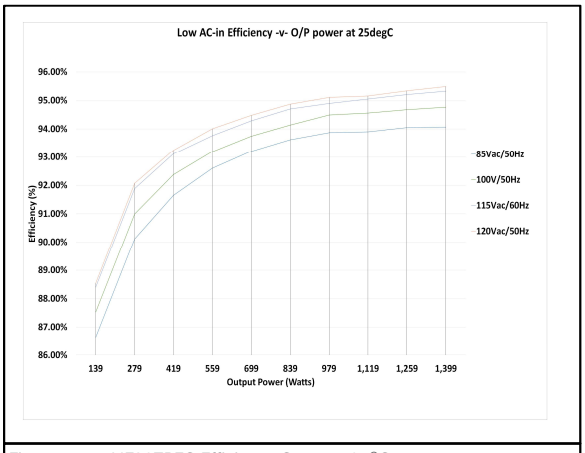


Figure 11: AIF06ZPFC Efficiency Curve @ 25°C
85Vac 100Vac 115Vac 120Vac
Loading: $P_{O,max}$= 1400W 10% increment to $P_{O,max}$

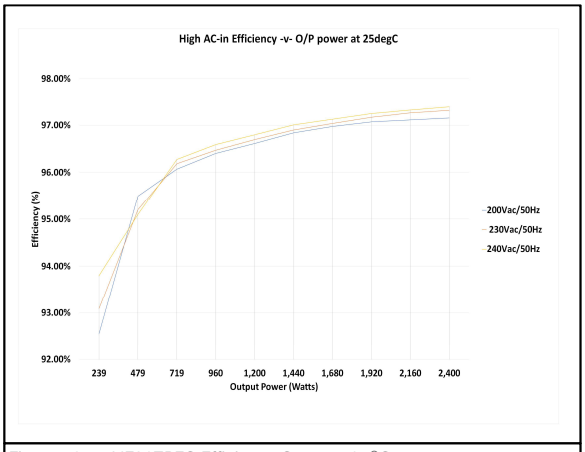


Figure 12: AIF06ZPFC Efficiency Curve @ 25°C
230Vac 200Vac 240Vdc
Loading: $P_{O,max}$ = 2400W 10% increment to $P_{O,max}$

ELECTRICAL SPECIFICATIONS

Protection Function Specifications

Input Fuse

The AIF06ZPFC series module do not have an in-line fuse fitted internally. In order to comply with CSA, VDE and UL safety regulations, it is recommended that a fuse of 250Vac, 25A max fast type per module.

Over Voltage Protection (OVP)

The over voltage point is 450Vdc (Typical). The power supply will be latched off. The OVP can be reset by toggling the PF Enable pin or using PMBus clear fault command if and only if the bulk voltage is lower than 390Vdc (Typical).

Parameter	Min	Typ	Max	Unit
V_O Output Overvoltage	445	450	455	Vdc

OVP Fault Status	
PFW	Low
LD Enable signal	Low when the bulk voltage drop to 292V (Typ) or low after 1.5s (Typ) if the bulk voltage is not lower than 292V (Typ)
Inrush by pass circuit (for 01L only)	Turn off at 290V (Typ) bulk voltage

Over Temperature Protection (OTP)

The power supply have a thermal sensor to monitor its internal temperature. If the module's internal temperature exceeds 108^{O}C (typical), the module will shut down itself, and auto recovery once internal temperature is less than 65^{O}C (typical).

OTP Fault Status	
PFW	Low
LD Enable signal	Low when the bulk voltage drop to 292V (Typ) or low after 1.5s (Typ) if the bulk voltage is not lower than 292V (Typ)
Inrush by Pass Circuit (for 01L only)	Turn off at 290V (Typ) bulk voltage

ELECTRICAL SPECIFICATIONS

Input Over voltage Protection (Input OVP)

An input overvoltage protection circuit protects the module under over input voltage conditions. PFC modules will be off when the input exceeds 305Vac with 500ms validation time. The PFC will auto recovery when the input is lower than the 270Vac.

Input OVP Fault status	
PFW	Low
LD Enable signal	Low after 1.5s (Typ) if the bulk voltage is not lower than 292V (Typ)
Inrush by pass circuit (for 01L only)	Turn off at 290V (Typ) bulk voltage

Input Under voltage Protection (Input UVP)

An input under voltage protection circuit protects the module under low input voltage conditions. Hysteresis is built into the PFC series module to allow for high levels of variation on the input supply voltage without causing the module to cycle on and off. PFC modules will operate when the input exceeds 81.5Vac (Typ) and turn off when input below 73.0Vac (Typ). For the AC cycling or missing cycle, the under voltage fault will be triggered if the brown out condition is longer than 500ms.

Input UVP Fault status	
PFW	Low at 340V default value or low after 500ms UV fault (Typ)
LD Enable signal	Low when the bulk voltage drop to 292V (Typ) or low after 1.5s (Typ) if the bulk voltage is not lower than 292V (Typ)
Inrush by pass circuit (for 01L only)	Turn off at 290V bulk voltage (Typ)

ELECTRICAL SPECIFICATIONS

Output Under voltage Protection

The under output protection is triggered if the bulk voltage is lower than 292V (Typ). LD enable will be activated low.

Output UVP Fault status	
PFW	Low at 340V default value
LD Enable signal	Low when the bulk voltage drop to 292V (Typ) or low after 1.5s (Typ) if the bulk voltage is not lower than 292V (Typ)
Inrush by pass circuit (for 01L only)	Turn off at 290V bulk voltage (Typ)

Over Current Protection (OCP)

The AIF06 series have the current monitor function to protect the unexpected over loading condition. Once the OCP is triggered, the module will be off and disable the load via LD enable signal. It is important that the loading of the AIF06 series shall be controlled by LD enable. The latency between LD signal and the load off response should be less than 10ms. Otherwise, the inrush resistors inside the modules may be stressed. AIF06 is a kind of traditional PFC which the input sources is in series with the output. It is not supported to the output short circuit. The output loading over the rating in the absolute maximum ratings section might cause the module damage.

Module	OCP Warning (Typ)	OCP (Typ)	OCP Validation Time (Typ)	Fault mode
01L	>6.2A at HL >3.7A at LL	>7.2A default at HL >4.2A default at LL	250ms at HL 150ms at LL	Latched at HL Auto recovery at LL
02L	>6.2A at HL >3.7A at LL	>7.2A default at HL >4.2A default at LL	250ms at HL 250ms at LL	Latched at HL Auto recovery at LL

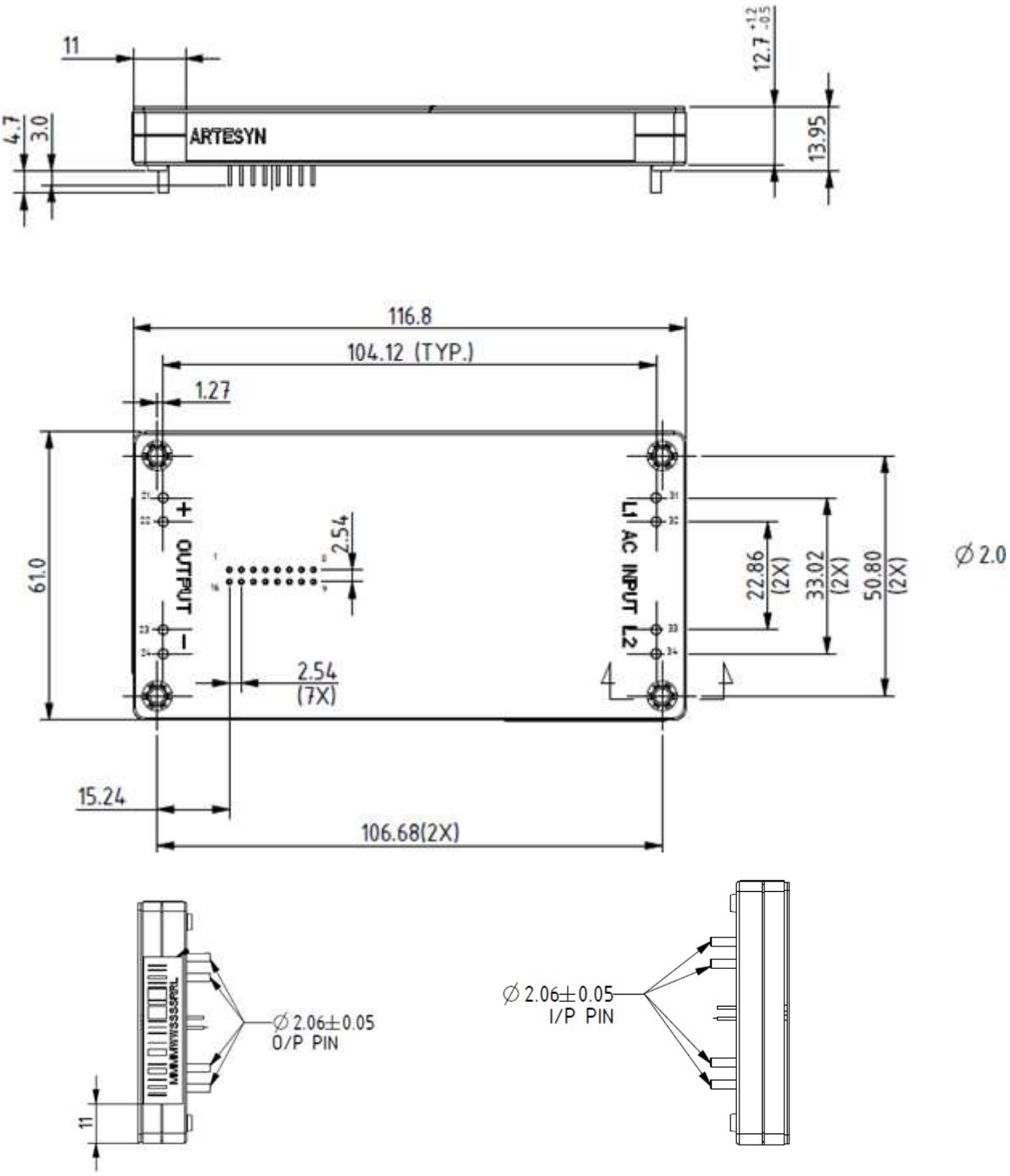
OCP Fault Status	
PFW	Low
LD Enable signal	HL: Low at bulk voltage 292V (1s delay if the bulk voltage is not lower than 292V) LL: Low after OCP fault
Inrush by Pass Circuit (for 01L only)	HL: Turn off at 290V bulk voltage LL: Turn off with LD

Fault during Parallel Mode Operation

External circuit/MCU shall be needed to switch off all the modules whenever one of the modules is in the fault condition. By monitoring each LD/PFW signal among the modules, whenever one of the LD/PFW signal is not good, the remaining modules shall be off immediately and reset all of the modules into the startup sequence state via toggling the PF Enable pin. For the parallel mode fault happened, it is important to synchronize the modules on/off sequence to prevent undesired condition. Detail please refer to PF Enable pin and the External Interruption circuit section.

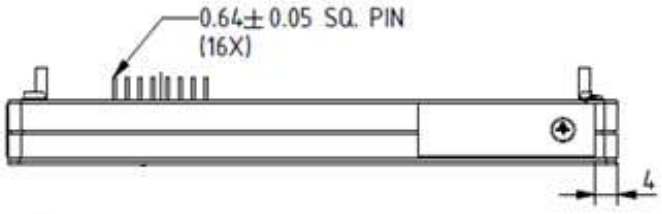
MECHANICAL SPECIFICATIONS

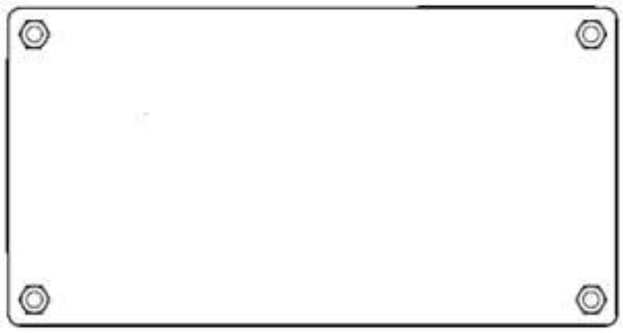
Mechanical Outlines (unit: mm)

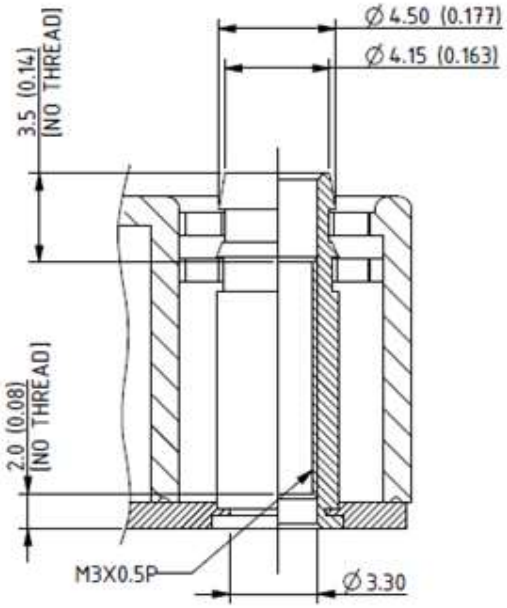


MECHANICAL SPECIFICATIONS

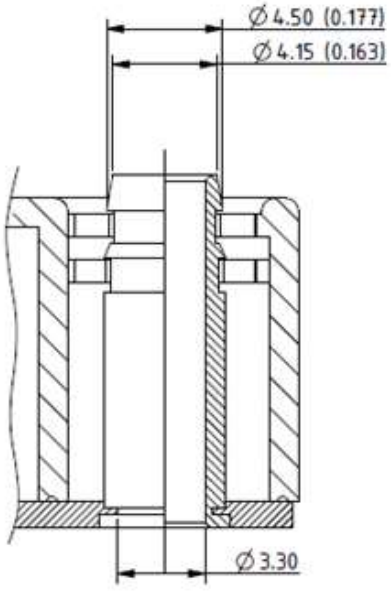
Mechanical Outlines (unit: mm)







THREADED INSERT



NON THREADED INSERT

MECHANICAL SPECIFICATIONS

Mechanical Outlines

Model Number	Stand off Options
AIF06ZPFC-02NTL	3.3mm hole, no thread
AIF06ZPFC-01NTL	3.3mm hole, no thread
AIF06ZPFC-02L	M3X0.5P thread
AIF06ZPFC-01L	M3X0.5P thread

Notes:

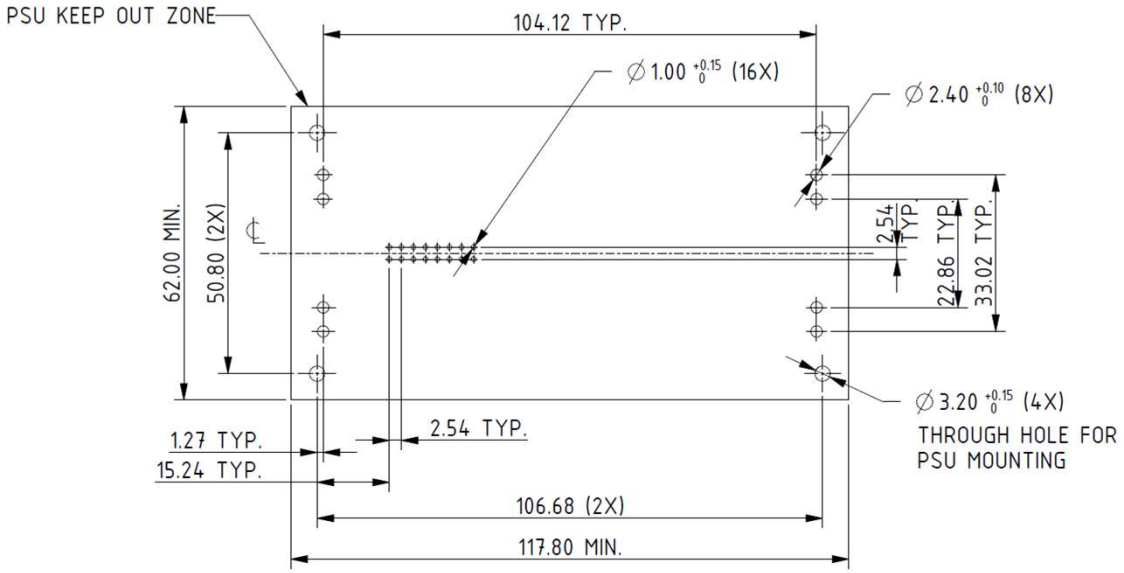
Surface flatness: Concave inwards: 0.2mm MAX

Convex outwards: 0.38mm MAX

Unless otherwise specified: Tolerance as below:

Whole Number	Decimal	Angle
+/-1	X +/- 0.5	+/- 0.5°
	XX +/- 0.25	

RECOMMENDED P.C.BOARD LAYOUT
(ALL HOLES DIAMETER ARE FINISHED WITH PLATING)



MECHANICAL SPECIFICATIONS

Pin Assignments

Pin Assignments		
Input (AC)	Output (DC)	Control Pin
31. L1	21. Vout+	1. PV AUX-
32. L1	22. Vout+	2. TEMP MON
33. L2	23. Vout-	3. C MON
34. L2	24. Vout-	4. C SHARE
		5. CLK OUT
		6. CLK IN
		7. PV AUX+
		8. SDA
		9. SCL
		10. I2C ADDRESS*
		11. V ADJ
		12. PFW ADJ
		13. S GND
		14. PFW
		15. LD ENABLE
		16. PF ENABLE

Note* - I2C ADDRESS signal pin supports both I2C address setting and phase shift setting.

MECHANICAL SPECIFICATIONS

Weight

The AIF06ZPFC series module weight is 9.4oz / 266g typical and 11.3oz / 320g maximum.

ENVIRONMENTAL SPECIFICATIONS

Safety Certifications

The AIF06ZPFC series module is intended for inclusion in other equipment and the installer must ensure that it is in compliance with all the requirements of the end application. This product is only for inclusion by professional installers within other equipment and must not be operated as a stand alone product.

Table 4. Safety Certifications for AIF06ZPFC Series Module

Standard	Agency	Description
UL 62368-1, 2nd Ed, 2014-12-01, CAN/CSA C22.2 No. 62368-1-14, 2nd Ed	UL+CUL	US and Canada Requirements
EN 62368-1:2014/A11:2017	TUV	Europe Requirements
EN 62368-1:2014/A11:2017	CE	CE Marking by Internal Verification/Certificate

ENVIRONMENTAL SPECIFICATIONS

EMI Emissions

The AIF06ZPFC series module will require additional EMI filtering to enable the system to meet relevant EMI standards. PFC modules have an effective input to ground (baseplate) capacitance of 1300pF maximum. This should be accounted for when calculating the maximum EMI 'Y' capacitance to meet ground leakage current specifications. An example filter circuit is shown below. EMI filter shielding may be required for better EMI performance.

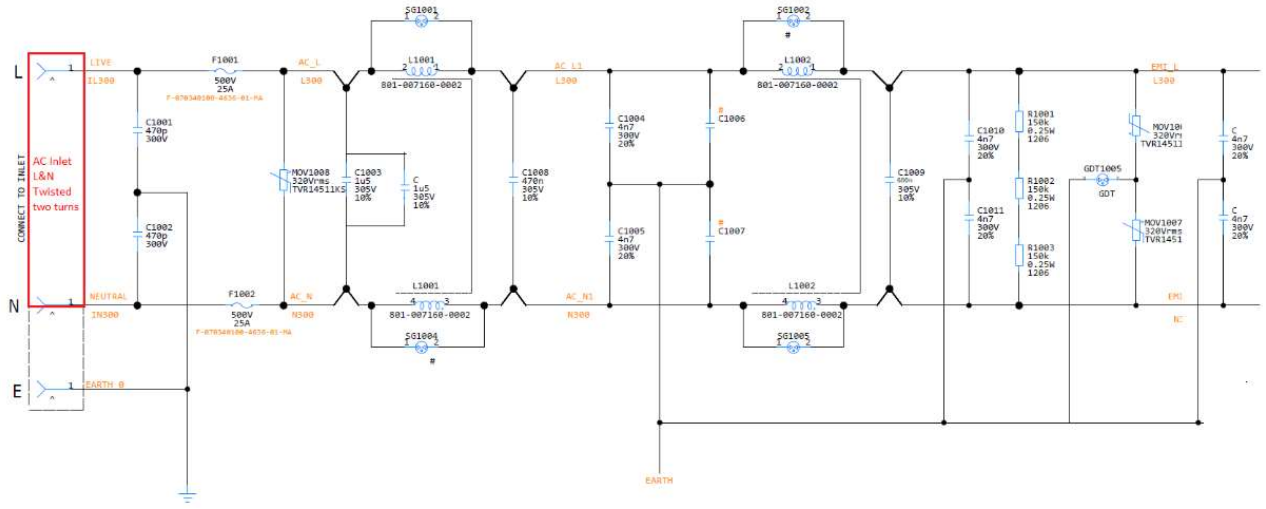


Figure 13: Reference EMI Filter Circuit – Filter 1 (Single AIF06ZPFC series module)

Single Module Enhanced Performance EMI filter

With additional filter change, it can increase around 3dB margin comparing with filter 1 above (Figure 13).

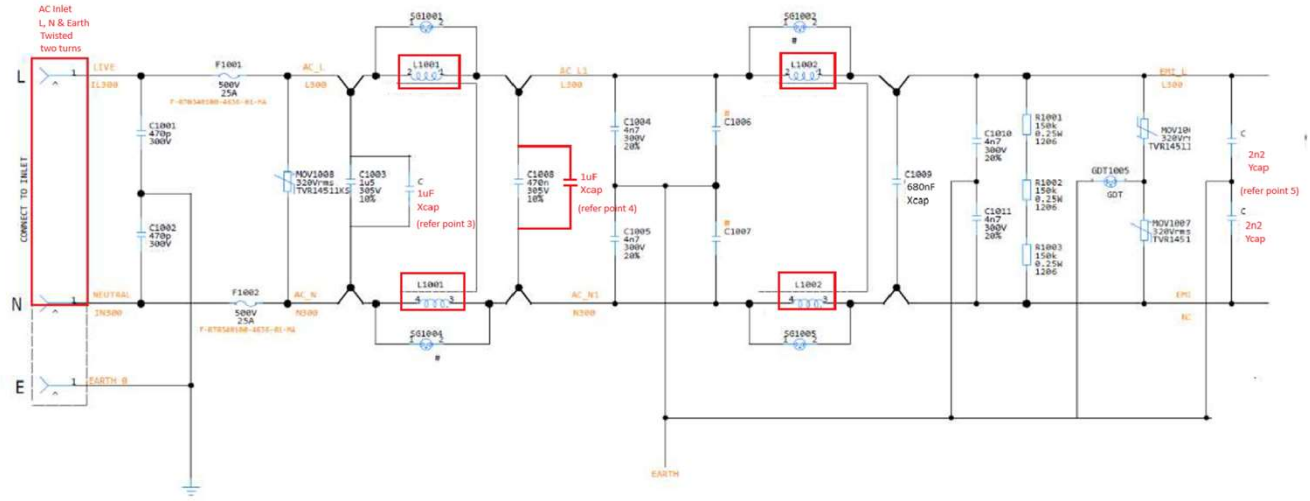


Figure 14: Enhanced Performance EMI Filter Circuit - Filter 2 (Single AIF06ZPFC series module)

ENVIRONMENTAL SPECIFICATIONS

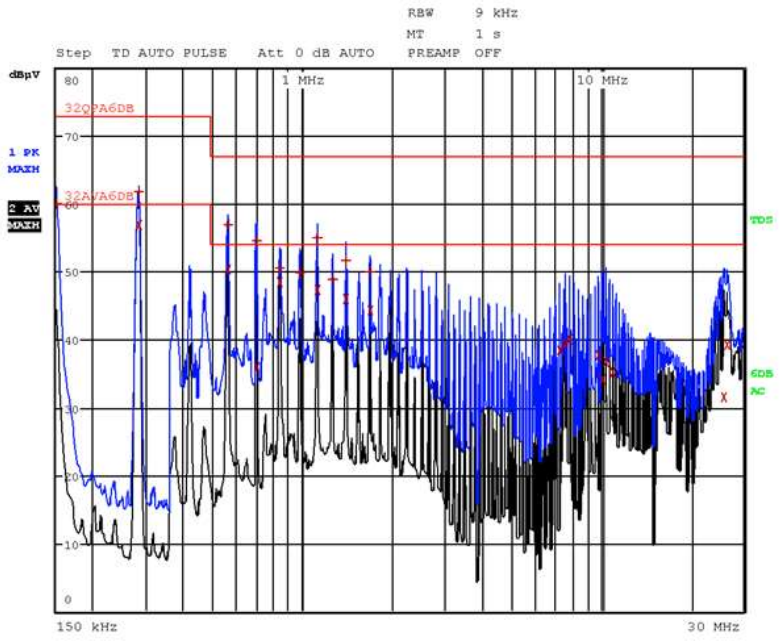


Figure 15: Conducted Emissions - Filter 1 (Single AIF06ZPFC series module)

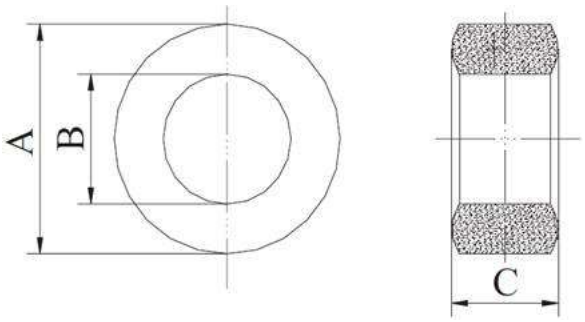
Single Module EMI Filter Component MPN List

Component	Filter 1	Filter 2 (Enhanced Performance EMI filter)
C1001, C1002	470 pF, TDK-CS75-B2GA471KYVKA	
F1001, F1002	LITTELFUSE-0505025.MXEP	
MOV1006 , MOV1007 , MOV1008	THINKING-TVR14511KSF	
C1003	1.5 uF, HUA JUNG COMPONENTS-MKP-155K0305AB1221	
X Cap parallel C1003 (refer point 3)	1.5 uF, HUA JUNG COMPONENTS-MKP -155K0305AB1221	1 uF, HUA JUNG COMPONENTS-MKP - 105K0305AB1221
L1001	Refer below	
C1008	470 nF, HUA JUNG COMPONENTS-MKP-474K0305AB1151-P	
X Cap Parallel C1008 (refer point 4)	----------	1 uF, HUA JUNG COMPONENTS MKP-105K0305AB1221
C1004 , C1005 , C1010 , C1011	4.7 nF, TDK-CS11ZU2GA472MYVKA	
L1002	Refer below	
C1009	680 nF, HUA JUNG COMPONENTS-MKP-684K0305AB1151-P	
R1001, R1002 , R1003	KOA-RK73H2BTTD1503F	
GDT1005	SANKOSHA-Y08SV-312BTR	
Y-Cap on MOV1001 (refer point 5)	4.7 nF, TDK-CS11ZU2GA472MYVKA	2.2 nF, TDK-CS80ZU2GA222MYVKA
MOV1001	THINKING-TVR14511KSF	

ENVIRONMENTAL SPECIFICATIONS

L1001, L1002		
	Filter 1	Filter 2 (Enhanced Performance EMI Filter)
Toroid	TL10	TL7
Turn Ratio	15:15	19:19
Magnet Wire Gauge (mm)	Dia: 1.4	Dia: 1.15
Dimension(mm) [refer figure below]	A=25; B=15; C=15	A=31; B=19; C=13

Toroid Dimension:



ENVIRONMENTAL SPECIFICATIONS

The AIF06ZPFC Series Module Filter Circuit for 2 units

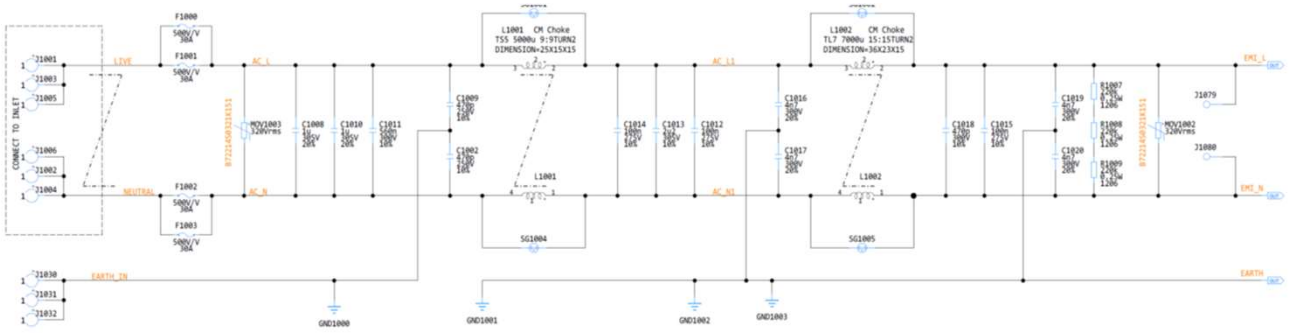


Figure 16: Reference EMI Filter Circuit (2 AIF06ZPFC series modules)

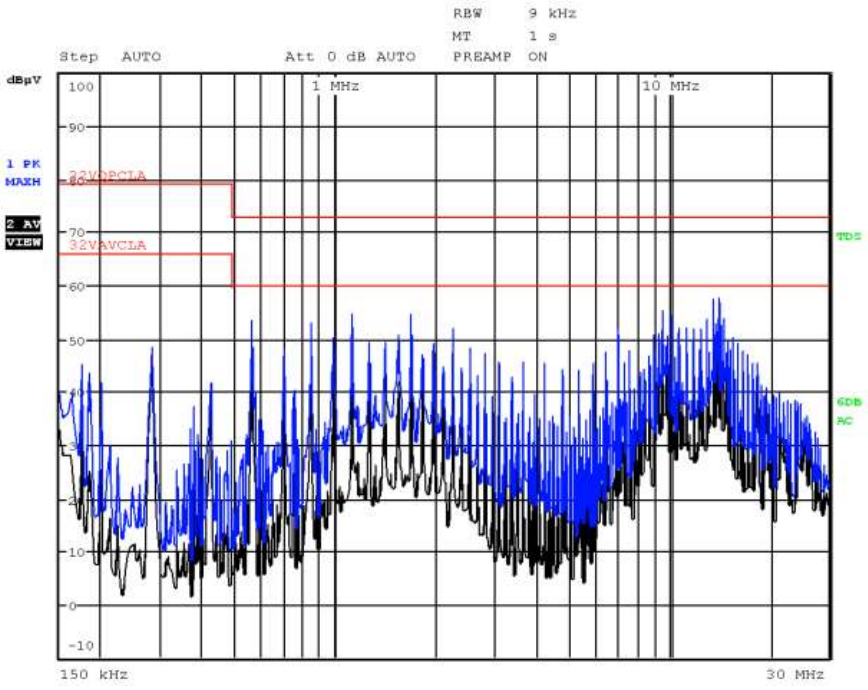


Figure 17: Conducted Emissions (2 AIF06ZPFC series modules)

ENVIRONMENTAL SPECIFICATIONS

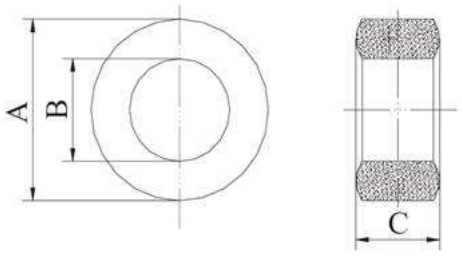
2 Modules EMI filter Component MPN List

Component	MPN
F1000, F1001, F1002, F1003	LITTELFUSE-0505030.MX52LEP
MOV1003, MOV1002	TDK - EPCOS-B72214S0321K151
C1008, C1010	TDK - EPCOS-B32923C3105M000
C1011	ISKRA SISTEMI-KNB1560 0.56UF 10% 300VAC L30 R22.5 DIM: 26.5X18.5X9 HF
C1009, C1002	MURATA - DE1B3KX471KN4AN01F
L1001	Refer below
SG1001, SG1002, SG1004, SG1005	MMC ELECTRONICS-DSP-201M-A21R
C1014, C1012, C1015	CARLI ELECTRONIC - PX104K3ID19H200D9R
C1013	TDK - EPCOS-B32924C3225K189
C1016, C1017, C1019, C1020	TDK - CS11ZU2GA472MYVKA
L1002	Refer below
C1018	TDK - EPCOS-B32923C3474K000
R1007, R1008, R1009	YAGEO - RC1206FR-07220KL

L1001	
Toroid	TS5
Turn Ratio	9:09
Magnet Wire Gauge (mm)	Dia: 1.6
Dimension(mm) [refer figure below]	A=25; B=15; C=15

L1002	
Toroid	TL7
Turn Ratio	15:15
Magnet Wire Gauge (mm)	Dia: 1.6
Dimension(mm) [refer figure below]	A=36; B=23; C=15

Toroid Dimension:



ENVIRONMENTAL SPECIFICATIONS

Storage and Shipping Temperature

The AIF06ZPFC series module can be stored or shipped at temperatures between -40°C to +110°C and relative humidity from 0 to 95%, non-condensing.

Humidity

The AIF06ZPFC series module will operate within specifications when subjected to a relative humidity from 0 to 95% non-condensing. The AIF06ZPFC series power supply can be stored in a relative humidity from 0 to 95% non-condensing.

:

POWER AND CONTROL SIGNAL DESCRIPTIONS

AC Input Pin

These pins provide the AC Mains to the AIF06ZPFC series module.

Pin 31 - AC Input Line / Return
Pin 32 - AC Input Line / Return
Pin 33 - AC Input Return / Line
Pin 34 - AC Input Return / Line

DC Output Pin

These pins provide the main output for the AIF06ZPFC series module. The "+" and the "-"pins are the output positive and output negative rails. The output (V_O) pins are electrically isolated from the power supply chassis.

Pin 21 - (+) 400V Output (Vo)
Pin 22 - (+) 400V Output (Vo)
Pin 23 - (-) 400V Output (Vo Return)
Pin 24 - (-) 400V Output (Vo Return)

Control Signals

The AIF06ZPFC series module contains a 16 pins control signal header providing an analogue control interface, temperature monitor and PFC module status warning interface.

PV AUX+ / PV AUX- - (pins 1,7)

PV AUX+ /PV AUX- provides an auxiliary power source for logic circuit. It supports 12V at 20mA. PV AUX+ and PV AUX- are isolated with power rail & signal ground, and the isolated voltage is 800V max. It can't support current share, and PV AUXs from different PFC modules cannot be directly tied together. External Oring diode connection method can be used to support PV AUX redundant application.

TEMP MON - (pin 2)

The TEMP MON pin provides an indication of the module's internal temperature. The voltage at the TEMP MON pin is proportional to the temperature of the module baseplate at 10mV per ^{O}C. Where:

Module temperature (^{O}C) = (V_TEMP_MON - 0.5) / 0.01

The temperature monitor signal can be used by thermal management systems (e.g. to control a variable speed fan). It can also be used for over temperature warning circuits and for thermal design verification of prototype power supplies and heatsink.

The temperature tolerance is +/5 ^{O}C to the temperature of the base plate.

POWER AND CONTROL SIGNAL DESCRIPTIONS

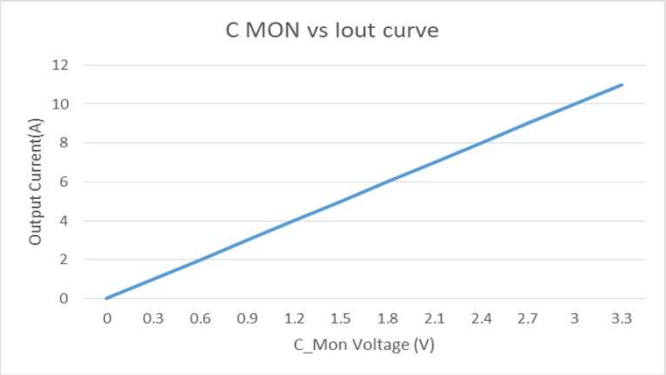
C MON - (pin 3)

The C MON pin provides an indication of the amount of current supplied by the module. The output of the C MON pin is a voltage source proportional to the output current of the module,

where $V_{C\ MON}$ / Io = 0.3V/A

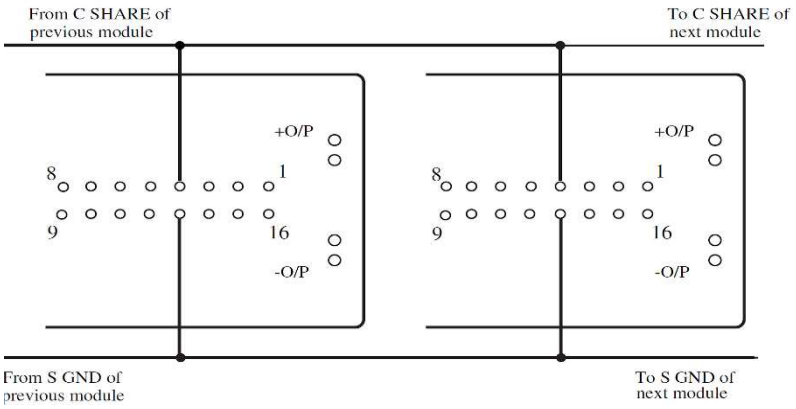
For example $V_{C\ MON}$ = 1.8V Typ at 6A load.

Maximum voltage on C MON is 3.3V and current higher than 10.5A can't be reflected by C MON. There is 10K ohm pull up resistor inside AIF06ZPFC series module for short circuit protection, and C MON pin can only be connected to high impedance external circuit.



C SHARE - (pin 4)

The C SHARE pins on each of the sharing group modules need to be connected together.



The voltage on the C SHARE pins represents the average load current per module. Each module compares this average with its own current and adjusts its output voltage to correct the error. In this way the module maintains accurate current sharing even under variable or light load conditions.

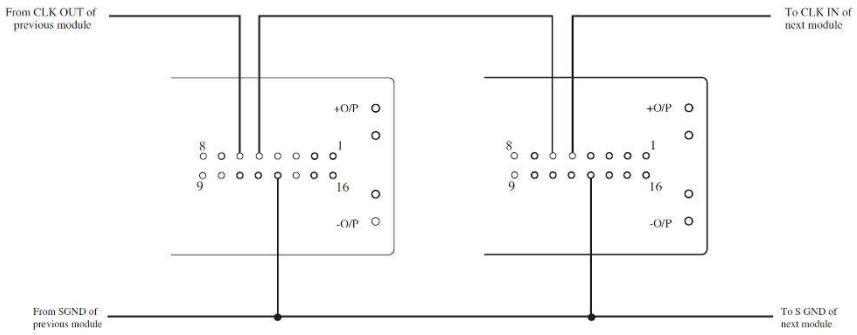
In multi-module paralleled systems, all modules will share current to within +/-0.6A of the average load current per module when the C SHARE pins of each module are connected together.

POWER AND CONTROL SIGNAL DESCRIPTIONS

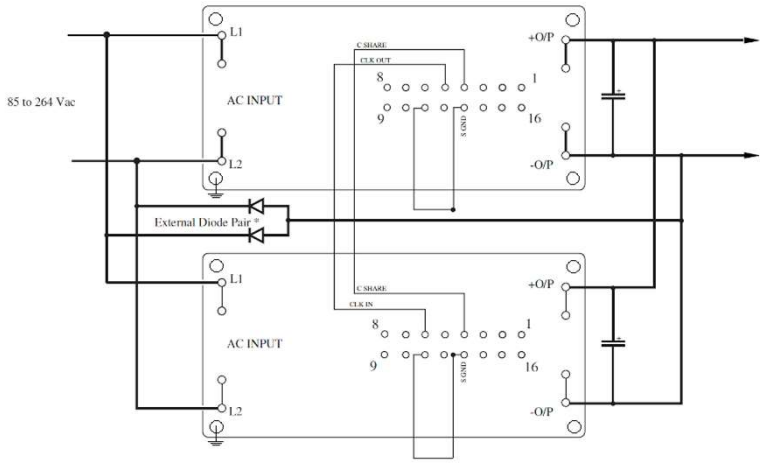
CLK IN, CLK OUT - (pins 5, 6)

The PFC's internal clock is accurate and stable over its full operating range and synchronization is not normally required but it can reduce noise & have better EMI performance in paralleled systems.

Clock signals can be wired in series (the CLK OUT pin of one module to the CLK IN pin of the next etc) in which case all the modules will be synchronized with the first module in the chain. Alternatively, an external clock signal of 3V3 logic level with duty cycle range (0.2 - 0.4) at 280KHz +/-5% can be connected to the CLK IN pins of all the modules.



Modules are synchronized by connecting the CLK OUT pin of one module to the CLK IN of the next module in an open daisy chain configuration. If the clock input to a module fails it will automatically revert to its internal clock and continue to operate at full power.



*External diode for AIF06ZPFC-02 is used. The current rating requirement of external rectifier for each line is 20A x number of units in parallel. For example, if there are 3 pieces of AIF06ZPFC-02 in parallel, customer will need to put 60A (20A x 3) external rectifier for each line.

For 01L, CLK Out signal will be generated after the internal MCU is initialized. Whereas for 02L , CLK Out signal will be generated in the AC brown in state with PF EN activated on. The 02L's CLK Out signal will be off when the bulk voltage is at 290V (Typ) or PF EN activated off. The CLK Out signal of the 02L shall be used for the external relay control feature. Detail please refer to AIF06ZPFC-02 Parallel Operation.

POWER AND CONTROL SIGNAL DESCRIPTIONS

SDA - (pin 8)

Serial data line in 3V3 logic. Connect to external host and/or to other AIF06ZPFC series module. A 2.2K ohm pull-up resistor integrated internally.

SCL - (pin 9)

Serial clock line in 3V3 logic. Connect to external host and/or to other AIF06ZPFC series module. A 2.2K ohm pull-up resistor integrated internally.

I2C ADDRESS - (pin 10)

The I2C ADDRESS pin supports both PMBus module address selection and phase shift features when communicating with multiple PMBus modules.

For multiple modules connecting in paralleled configuration (or current sharing group), phase shift setting is recommended to be used in the application in order to optimize the application performance. When there's no CLK IN signal input or the CLK IN frequency is out of the operating range, the module will use its defaulted clock frequency to generate a phase shift clock frequency at CLK OUT signal pin.

CLK OUT and CLK IN pins are in daisy chain. However, the phase shift proper operation is only be established at the first start-up with correct CLK IN delay setting between modules, otherwise synchronization with phase setting won't be successful. Other than the phase shift angle setting, the CLK IN read delays setting are also listed into the table below. Module to module daisy chain setting sequence is important, the master module will be set 0 delay, the first slave module will be set 100ms delays, the second slave module will be set 200ms .., etc.

Each module generates CLK OUT frequency output after detecting the CLK IN frequency & phase shift angle setting. Open connection or an external clock 280KHz can be set at CLK IN signal pin of the master module for daisy chain multiple modules' operation. AIF06ZPFC series module switching frequency with two interleaved phases inside the module is half of the clock frequency. Please refer to phase shift & delays selection table below.

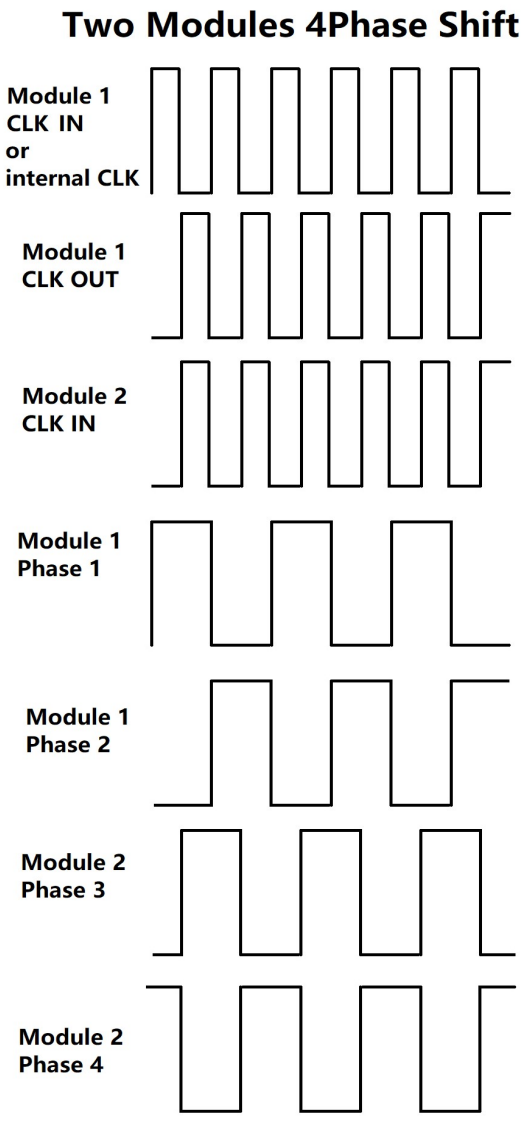
POWER AND CONTROL SIGNAL DESCRIPTIONS

Paralleled Module Number	R_Address (Ohm)	Address	Phase Shift between Module Clock Signals (deg)	Actual Phase Shift (deg)	CLK IN Sensing Delay from the first module (ms)
2	0	B0	180	0, 180	0
	348	B2	180	90, 270	100
3	715	B4	120	0, 180	0
	1130	B6	120	60, 240	100
	1540	B8	120	120, 300	200
4	2000	BA	90	0, 180	0
	2490	BC	90	45, 225	100
	3010	BE	90	90, 270	200
	3650	C0	90	135, 315	300
5 or above	4320	C2	72	0,180	0
	4990	C4	72	36, 216	100
	5760	C6	72	72, 252	200
	6650	C8	72	108, 288	300
	7680	CA	72	144, 324	400
	8660	CC	72	180, 0	500
	10000	CE	72	216, 36	600
5 or above	11500	D0	72	252, 72	700
	13000	D2	72	288, 108	800
	15000	D4	72	324, 144	900
Additional group with 2 modules	17400	D6	180	0, 180	0
	20000	D8	180	90, 270	100
Additional group with 3 modules	23200	DA	120	0, 180	0
	27400	DC	120	60, 240	100
	33200	DE	120	120, 300	200
Additional group with 4 modules	40200	E0	90	0, 180	0
	49900	E2	90	45, 225	100
	64900	E4	90	90, 270	200
	88700	E6	90	135, 315	300
Additional group with 2 modules	140000	E8	180	0, 180	0
	280000	EA	180	90, 270	100
1	Open	EC	90	0, 90	0

POWER AND CONTROL SIGNAL DESCRIPTIONS

For example of two modules in paralleled configuration. Module1 I2C address is set to B0 (resistor is 0 ohm), module2 I2C address is set to B2 (resistor is 348 ohm). Module1 CLK OUT signal is $360^{O}/2$ (in paralleled module number) $=180^{O}$ phase shift of module1 CLK IN signal. 280KHz CLK IN signal is internally split to two interleaved PWM phases, each phase PWM frequency is 140KHz. Since module's CLK IN and CLK OUT pins are daisy chain, the module 2 CLK IN is 180^{O} phase shift of module 1 CLK IN. The 4 phases of two modules are $360^{O}/4 = 90^{O}$ phase shift.

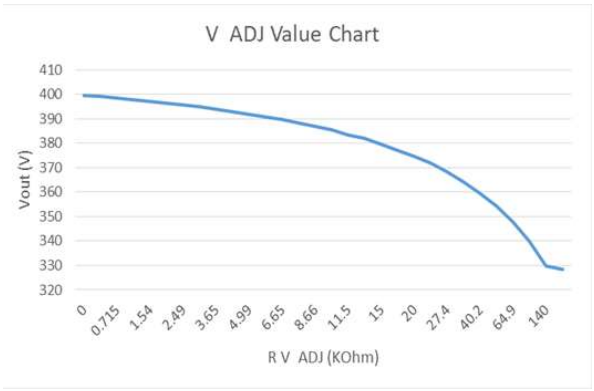
There is 2N PWM phases with N multiple module paralleled configuration. The phase shift between modules CLK IN is $360^{O}/N$, and the 2N phase is $360^{O}/2/N$ phase shift. Due to MCU limitation, the max N is 5, if N is higher than 5 (up to 10), the module CLK IN phase shift will be clamped to $360^{O}/5 = 72^{O}$.

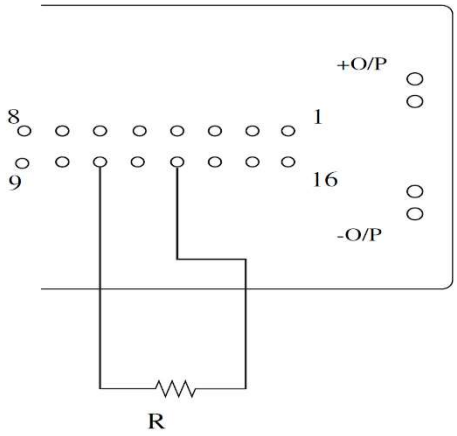


POWER AND CONTROL SIGNAL DESCRIPTIONS

V ADJ - (pin 11)

The output voltage of the AIF06ZPFC series module can be accurately adjusted from 330V to 400V. Adjustment can be made using a 0.1% resistor connected as below





Vo = 291.4* (R+80.45) / (R+59.9) + 8.34

Where R is the resistor connected between the Vadj pin to S GND (units in Kohm)

Examples 385V set with R_Vadj = 11K ohm 330V set with R_Vadj = 150K ohm

PFW ADJ (Power Fail Warning Adjust) - (pin 12)

The level at which a Power Fail Warning occurs can be programmed using the PFW adjust input or via PMBus command. If the pin is left unconnected then the PFW operates at the 340V default factory set value. The output from the PFW ADJ pin is a 1mA current source. To adjust the PFW threshold, a voltage source (0 - 4V) or a programming resistance (0 - 4K ohm) referenced to S GND (pin 13) should be connected. This allows adjustment of the PFW threshold from 307V up to 340V.

POWER AND CONTROL SIGNAL DESCRIPTIONS

S GND - (pin 13)

The S GND pin internally connected to the -O/P terminals via a 1.5 ohm resistor. And, it's mainly used for VADJ, PFW ADJ and and I2C ADDRESS / phase shift resistor setting as a reference GND on each of the PFC modules, and can be separated or disconnected for parallel application.

Note: Recommend no connection between S GND and Vout- power return on external circuit.

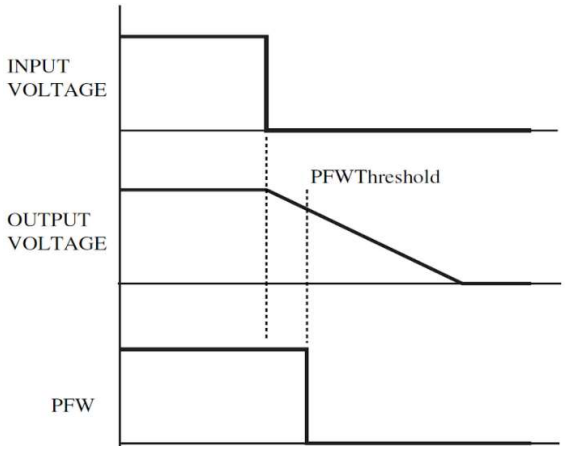
In paralleled operation, short each AIF06ZPFC's S GND together.

PFW - (pin 14)

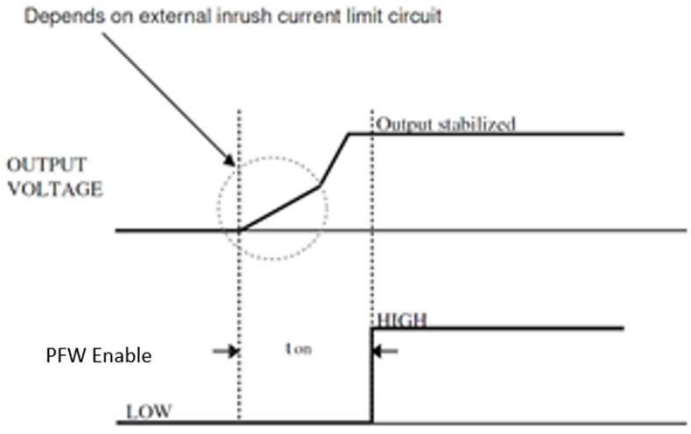
PFW (Power Fail Warning) pin output a signal that can drive a LED to provide the power fail warning of the unit. When the output voltage is out of regulation or faults (refer to the Protection Function Specifications) are detected, this signal will go from high to low.

The output of the PFW signal can drive an opto-coupler to provide an isolated signal from the primary side to the secondary side. The normal factory set PFW threshold is set at 307V to 340V via PFW ADJ resistor or via PMBus command (refer to PMBus section). The PFW will be recovered if the bulk voltage is 10V greater than the PFW threshold before LD go to low. (refer to PMBus section).

PFW (Bit 1) reporting under STATUS_MFR_SPECIFIC (80h) is based on PFW.



When the PFC power up, the PFW is high once the output is in regulation.

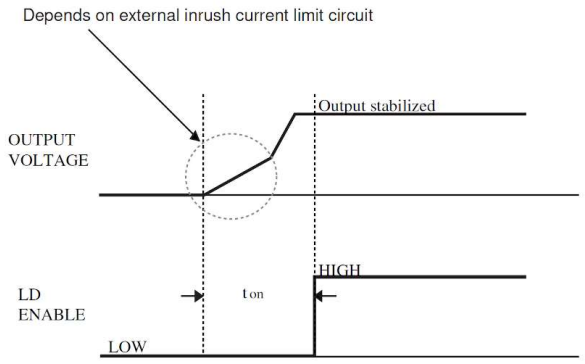


POWER AND CONTROL SIGNAL DESCRIPTIONS

LD ENABLE - (pin 15)

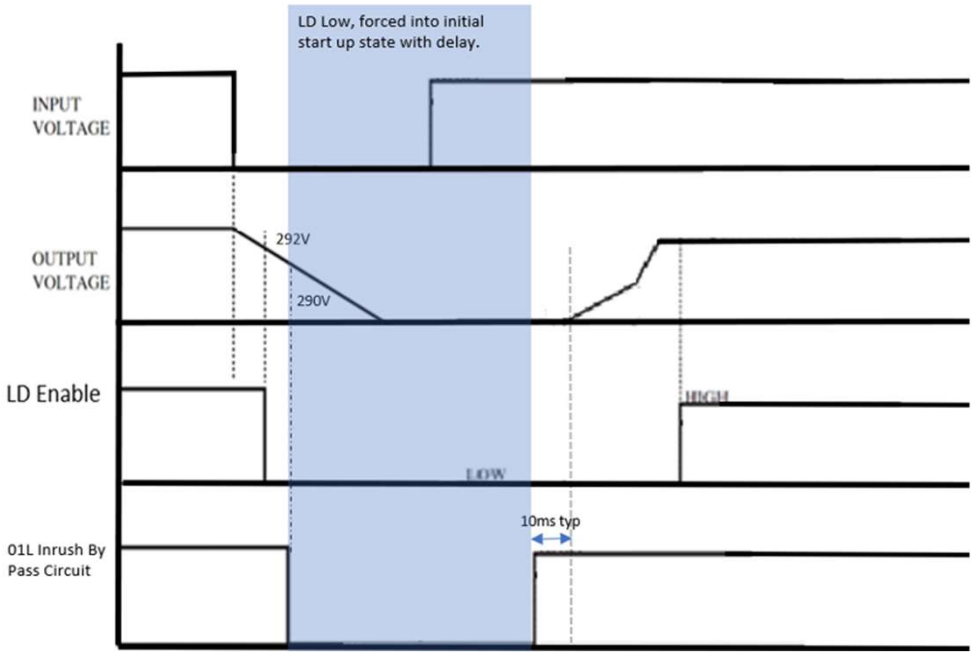
After the PFC power up sequence, the power to the load can be enabled, and the PFC can automatically enable the load using the LD ENABLE signal.

LD_DISABLE (Bit 0) reporting under STATUS_MFR_SPECIFIC (80h) is based on LD ENABLE.



Similar with PFW, the LD signal can drive an opto-coupler to provide an isolated signal from the primary side to the secondary side. The LD voltage sensing threshold is set at 292Vdc (Typ). Once the LD is lower than the threshold, the modules will be forced into the initial PFC start up sequence. For 01L only, the internal by pass circuit will be off at bulk voltage 290Vdc (Typ).

For the faults (refer to the Protection Function Specifications) are detected, this LD Enable will override the 292Vdc (Typ) voltage sensing condition.



POWER AND CONTROL SIGNAL DESCRIPTIONS

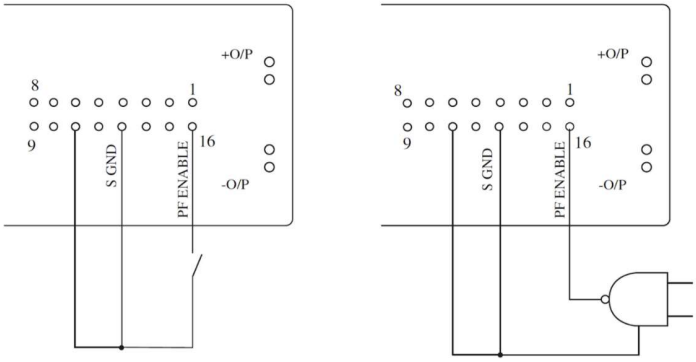
PF ENABLE - (pin 16)

The PF ENABLE pin is a TTL compatible input used to turn the output of the module on or off.

For module with no suffix, the output is enabled when the PF ENABLE is open or driven to a logic high > 2.2V. The output is disabled when the PF ENABLE is connected to S GND or driven to a logic low of < 0.8V (but not negative).

For module with suffix “N”, the output is enabled when the PF ENABLE is connected to S GND or driven to a logic low < 0.8V (but not negative). The output is disabled when the PF ENABLE is open or driven to a logic high > 2.2V.

PF ENABLE (Bit 2) reporting under STATUS_MFR_SPECIFIC(80h) is based on PF ENABLE.



The PF ENABLE pin can be as an interrupt function pin for the Parallel Operation feature. It can reset the faults and force the modules into initialize start up state. Application can refer to the section of External Control Options.

MCU Internal Flash Memory

The module is equipped with a 16K byte flash memory. This device will be programmed during the manufacturing process. The EEPROM content will include the following information:

-Manufacturer name string “Artesyn”
-Product name and product number
-Serial number assigned by manufacturer
-Max output power

PMBUS™ SPECIFICATIONS

AIF06PFC Support PMBus™ Command List

The AIF06PFC series module is compliant with the industry standard PMBus™ protocol for monitoring and control of the power supply via the I2C interface port. PEC is supported, PMBUS™ clock speed supports up to 400Kbps.

PMBus™ specification revision is 1.2 and SMBus™ specification revision is 2.0.

URL to PMBus™/SMBus™ Org specifications: http://pmbus.org/specs.html and http://smbus.org/specs/

AIF06PFC Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
01h	OPERATION**	80	R/W	1	-	Enable/disable, margin settings. Immediate off, nominal margin
03h	CLEAR_FAULTS	-	W	-	-	Clears faults
12h	RESTORE_DEFAULT_ALL	-	W	0	-	Restores values to default store
15h	STORE_USER_ALL	-	W	0	-	Stores values to user store
20h	VOUT_MODE	1E	R	1	-	Scaling factor on voltage data for commanding or reading the output voltage
22h	VOUT_TRIM	0	R/W	2	Binary integer	Applies offset voltage to VOUT set-point within ±200 (±6.0V)
40h	VOUT_OV_FAULT_LIMIT	450V	R/W	2	Depends on VOUT_MODE	Sets the VOUT overvoltage fault threshold (290V to 450V)
42h	VOUT_OV_WARN_LIMIT	420V	R/W	2	Depends on VOUT_MODE	Sets the VOUT overvoltage warning threshold (290V to 440V)
43h	VOUT_UV_WARN_LIMIT	297V	R/W	2	Depends on VOUT_MODE	Sets the VOUT under voltage warning threshold(297V to 305V)
44h	VOUT_UV_FAULT_LIMIT	292V	R/W	2	Depends on VOUT_MODE	Sets the VOUT under voltage fault threshold(292V to 300V)
46h	IOUT_OC_FAULT_LIMIT	7.2A High 4.2A Low	R/W	2	Linear	Sets the IOUT over current fault threshold (0A to 4.2A at low line, 0A to 7.2A at high line
4Ah	IOUT_OC_WARN_LIMIT	6.7A high 3.9A Low	R/W	2	Linear	Sets the IOUT over current warning threshold (0A to 4.2A at Low Line,0A to 7.2A at High Line)
4Fh	OT_FAULT_LIMIT	108degC	R/W	2	Linear	Sets the over-temperature fault limit. (0degC to 108degC)
51h	OT_WARN_LIMIT	90degC	R/W	2	Linear	Sets the over-temperature warning limit. (0degC to 110degC)
55h	VIN_OV_FAULT_LIMIT	>305Vac	R/W	2	Linear	Sets input over-voltage fault limit (85Vac-305Vac)
57h	VIN_OV_WARN_LIMIT	>273Vac	R/W	2	Linear	Sets input over-voltage warning limit (85Vac to 305Vac)
58h	VIN_UV_WARN_LIMIT	<83Vac	R/W	2	Linear	Sets the VIN under voltage warning threshold(73Vac-84Vac)
59h	VIN_UV_FAULT_LIMIT	<73Vac	R/W	2	Linear	Sets the VIN under voltage fault threshold(70Vac to 73Vac)
60h	TON_DELAY	0	R/W	2	Linear	Sets the delay time from enable to VOUT Rise Range: 0 - 60000mS

PMBUS™ SPECIFICATIONS

AIF06PFC Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
64h	TOFF_DELAY	0	R/W		Linear*	Sets the delay time from DISABLE to start of VOUT fall Range: 0 - 60000mS
78h	STATUS_BYTE	-	R	1	-	First byte of STATUS_WORD
79h	STATUS_WORD	-	R	2	-	Summary of critical faults
7Ah	STATUS_VOUT	-	R	1	-	Reports VOUT warnings/faults
7Bh	STATUS_IOUT	-	R	1	-	Reports IOUT warnings/faults
7Ch	STATUS_INPUT	-	R	1	-	Reports input warnings/faults
7Dh	STATUS_TEMPERATURE	-	R	1	-	Reports temperature warnings/faults
7Eh	STATUS_CML	-	R	1	-	Reports communication, memory, logic errors
80h	STATUS_MFR_SPECIFIC	-	R	1		Reports I/O pin status
	b7:4 Reseved					This status will not set mfr bit in status word.
	b3 PFC_OFF					Report unit ON/OFF status. 1 - OFF 0 - ON
	b2 PF ENABLE					Report pin status of PF ENABLE (Pin 16) 1 - Enable 0 – Disable
	b1 PFW					Report pin status of PFW (pin 14) 1 - Active (Vout <PFW_ON_LIMIT) 0 – Inactive(Vout>PFW_OFF_LIMIT)
	b0 LD_DISABLE					Report pin status of LD ENABLE (Pin15) 1 - Disable 0 - Enable
88h	READ_VIN	-	R	2	Linear	Returns input voltage in Volts ac.
89h	READ_IIN	-	R	2	Linear	Reports input current measurement
8Bh	READ_VOUT	-	R	2	Depends on VOUT_MODE#	Reports output voltage measurement
8Ch	READ_IOUT	-	R	2	Linear	Reports output current measurement
8Dh	READ_TEMPERATURE_1	-	R	2	Linear	Reports internal temperature measurement
95h	READ_FREQUENCY	282	R	2	Linear	Reports actual switching frequency (KHz)
98h	PMBUS_REVISION	22	R	1	-	Reports the PMBus revision used
99h	MFR_ID	ARTESYN	BR	16	ASCII	Manufacturer identifier
9Ah	MFR_MODEL_ID	AIF06ZPFC-01L	BR	16	ASCII	Manufacturer model ID

PMBUS™ SPECIFICATIONS

AIF06PFC Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
9Bh	MFR_REVISION	BBBSSSHHHH	BR	10	ASCII	Manufacturer revision BBBSSSHHHH(BBB=bootloader version S= Application version, H =Hardware version, ASCII)
9Ch	MFR_LOCATION	-	BR	11	ASCII	Manufacturer location identifier
9Dh	MFR_DATE	YYMMDD	BR	6	ASCII	Manufacturer date
9Eh	MFR_Serial	-	BR	11	ASCII	Serial number : LLLYYWWSSSS Legend: LLL - MANUFACTURER LOCATION YY - MANUFACTURING YEAR WW - MANUFACTURING WEEK SSSS - SEQUENTIAL SERIAL ID
A0h	PFW_ON_LIMIT	<PFW ADJ	R/W	2	Linear	Sets the Power Failure Warning ON threshold When Vout < this limit, PFW will active Range: 307Vdc - 340Vdc
A1h	PFW_OFF_LIMIT	>(PFW ADJ+10V)	R/W		Linear	Sets the Power Failure Warning OFF threshold When Vout > this limit, PFW will inactive Range: 312Vdc - 345Vdc

Note:
*For linear mode:

The Linear Data Format is a two byte value with:

- An 11 bit, two's complement mantissa and
- A 5 bit, two's complement exponent (scaling factor).

The format of the two data bytes is illustrated in Figure 4.

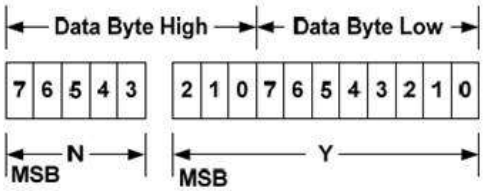


Figure 4. Linear Data Format Data Bytes

The relation between *Y*, *N* and the "real world" value is:

$X = Y \cdot 2^N$

Where, as described above:

X is the "real world" value;

Y is an 11 bit, two's complement integer; and

N is a 5 bit, two's complement integer.

Devices that use the Linear format must accept and be able to process any value of *N*.

PMBus™ SPECIFICATIONS

*For Vout_mode:

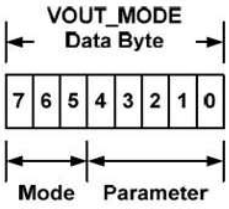


Figure 5. VOUT_MODE Command Data Byte Structure

If a device accepts the VOUT_MODE command, the Mode and Parameter are retained until changed with another VOUT_MODE command or until the bias power is removed.

Sending the VOUT_MODE command using the SMBus Read Byte protocol returns one byte with the Mode and Parameter as shown in Figure 5.

Table 2 shows the permitted values and format of the VOUT_MODE data byte. More information on the VOUT_MODE command is used with output voltage related commands is given below in Section 8.3.

Table 2. Summary Of The VOUT_MODE Data Byte Format

Mode	Bits [7:5]	Bits [4:0] (Parameter)
Linear	000b	Five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.
VID	001b	Five bit VID code identifier per
Direct	010b	Always set to 00000b

**For Operation (01H):

Only AIF06ZPFC-02 is supported broadcast function to control multiple units on/off at the same time.

Only operation command (01h) with write access is supported broadcast and read operation is unsupported.

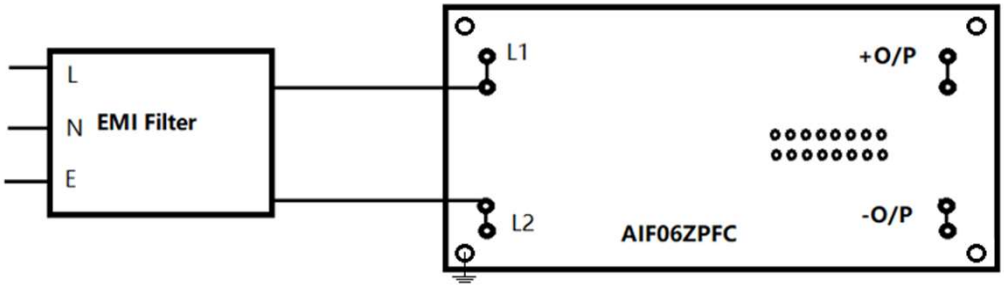
Address for broadcast is 0x00 (7bit address).

S	Slave address(7 bit address) 0x00	W 0	ACK	Operation command code 0x01	ACK	data 0x80	ACK	P

APPLICATION NOTES

PFC Module Input Connection Diagram

Below block diagram is the application connection of the AIF06ZPFC series module.

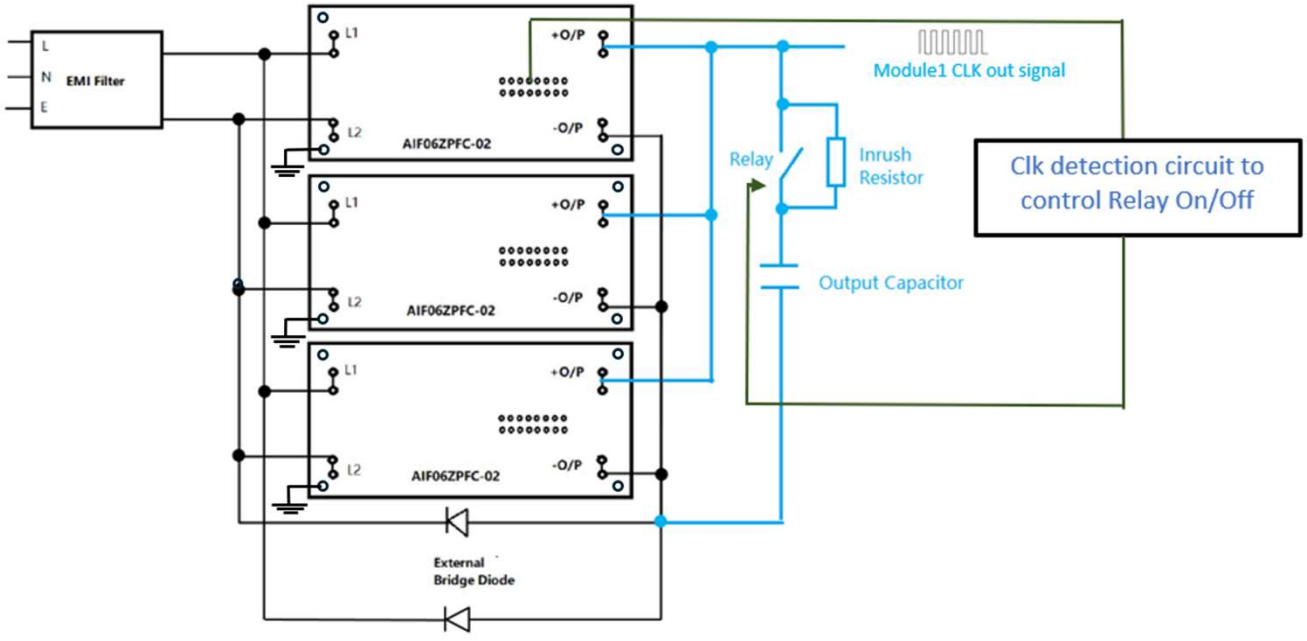


AIF06ZPFC-02 Parallel Operation

The AIF06ZPFC-02 has been specifically designed for paralleling applications where the total input current exceeds 40Arms. For stand-alone applications or those where the total input current does not exceed 40Arms, the AIF06ZPFC-01 is recommended.

The AIF06ZPFC-02 requires external negative rail rectifiers to be implemented at the input to the system. It is possible to operate the AIF06ZPFC-02 as a stand-alone configuration although the external negative rail rectifiers must still be provided.

The Inrush resistors shall be well selected basing on the peak inrush current limited requirement as well as resistors' power rating and not damage the module under any condition of load, temperature and input voltage including repeated, rapid cycling of the



Note: High current external bridge diode is recommended.

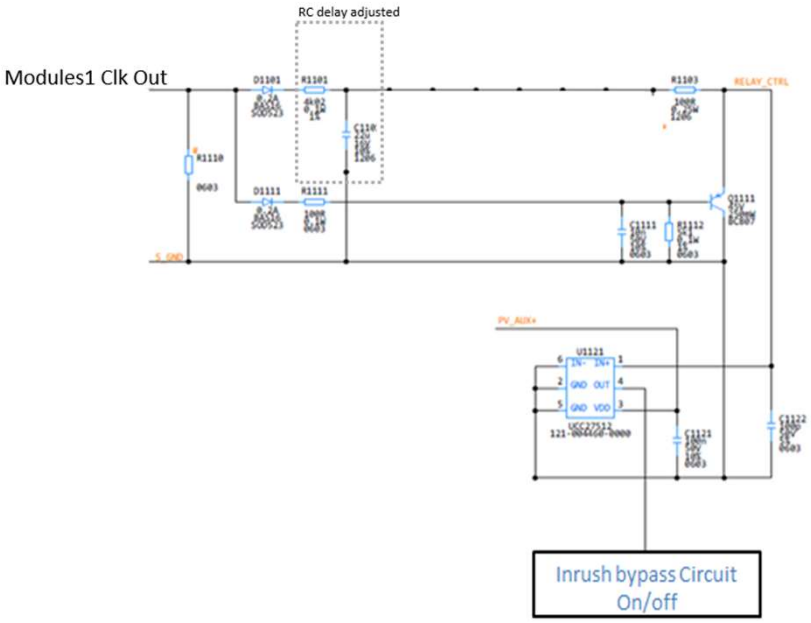
To reduce noise and for EMI purpose, the module should be earthed properly by connecting one of the module input side standoff to system's earth.

APPLICATION NOTES

The AIF06ZPFC-02L requires external relay to bypass the external inrush resistors. The relay turn on time should consider the factor of the bulk cap's charging time as well as the start up sequence of the modules. For those design using LD or PFW to control the external relay which is placed in front of the modules, it needs to be well evaluated whether any input voltage drop affects the modules' brown-in sensing, else modules may classify as brownout condition.

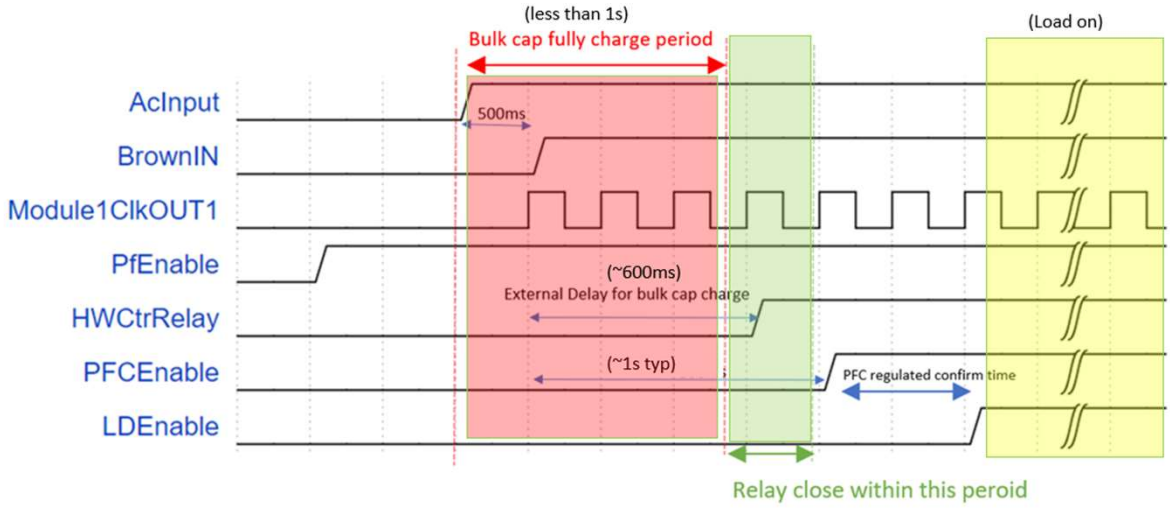
The AIF06ZPFC-02L has specific feature in the clkout pin. The clkout signal will be generated after the AC brown in is confirmed, whereas the clkout signal will be off once the bulk voltage is 290V or toggling the PF Enable pin. By detecting the clkout signal with external appropriated delay , the relay can be well controlled.

Circuit using clkout singal to control the external relay



The external delay is for the bulk cap fully charged by rectified AC. This can prevent a large inrush current induced when the relay is closed. The relay is suggested to be closed before the PFC start up.

External Relay Timing diagram

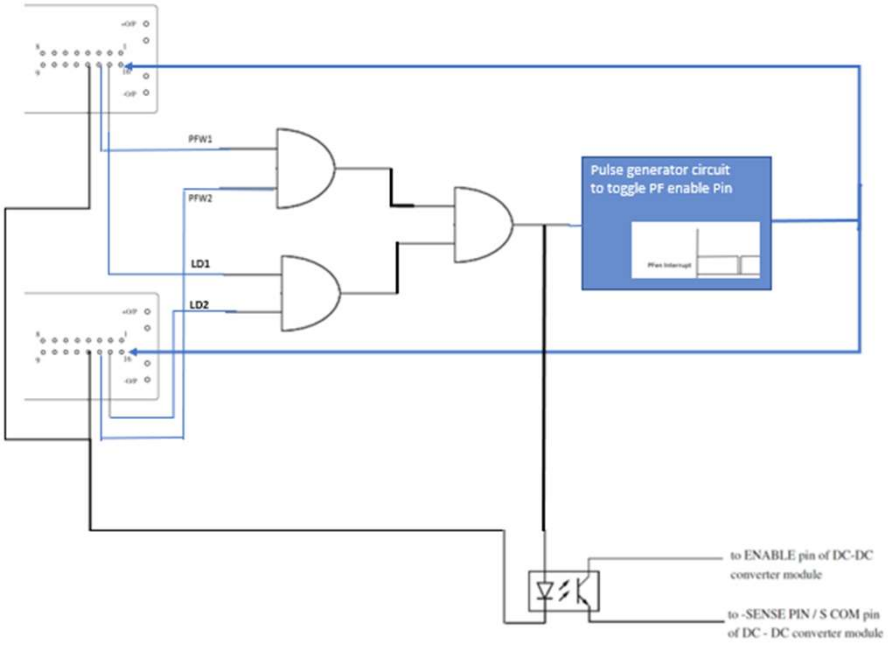


APPLICATION NOTES

AIF06ZPFC-01L External Interruption Circuit

Option 1:

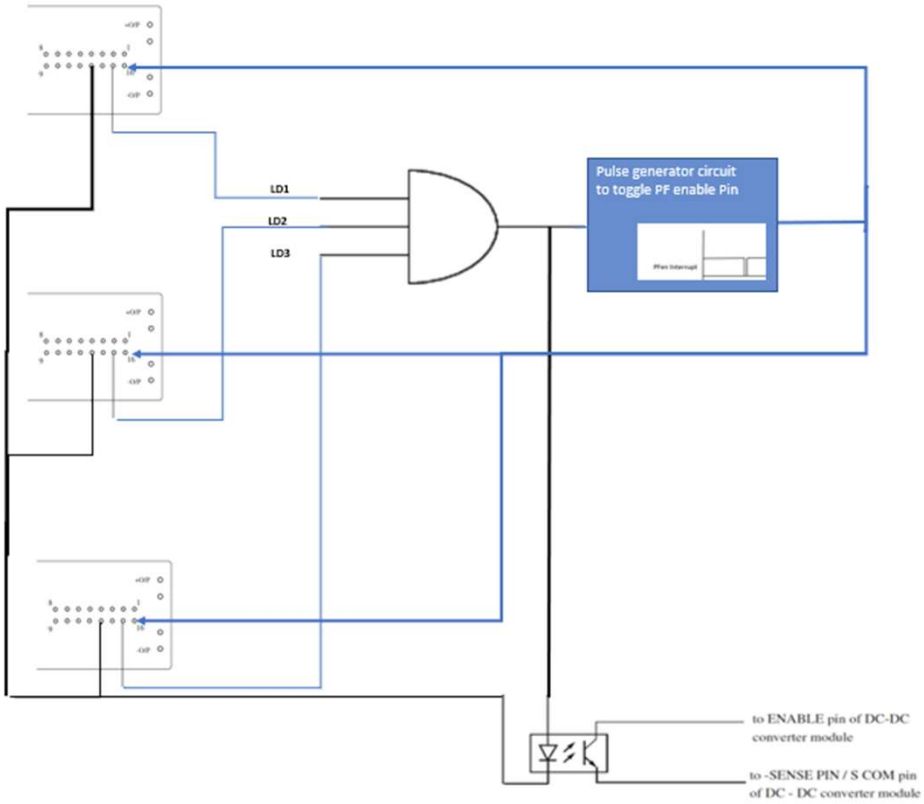
For 01L, the inrush circuit is inside the module. To prevent failure under Voltage Dips and Interruptions testing, one of the options shall be used for PF ENABLE OFF control. PFW shall be set to 322V or higher by changing the voltage of PFW ADJ or PFW on_Limit of the PMBus to limit the surge current during AC recycling. The PFW/LD signals of the paralleled modules shall be combined with the Logic. The interrupt circuit will toggle the PF_EN pin so that all the modules are forced into the initial start up state.



Option 2:

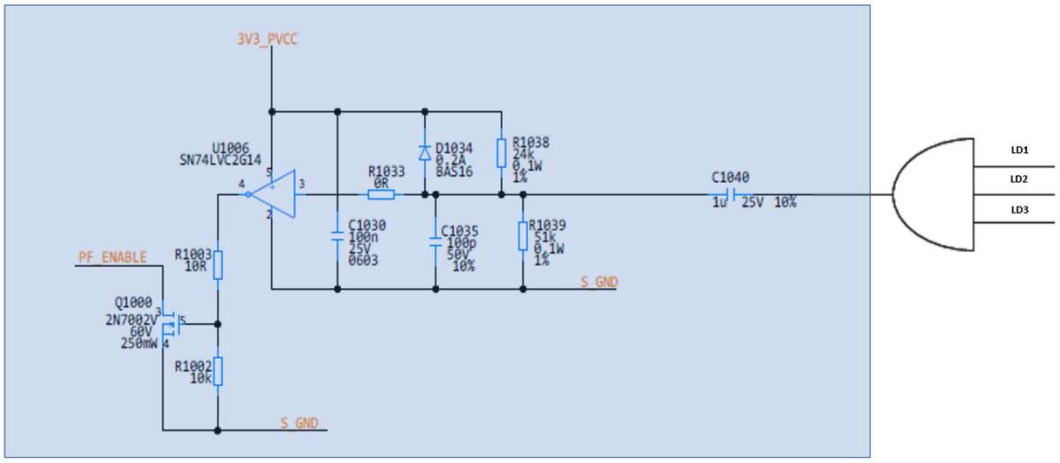
External MCU logic scheme (either use Bulk monitor signal or PFW signal) and set PF ENABLE off at 322V or higher for the paralleled modules.

APPLICATION NOTES

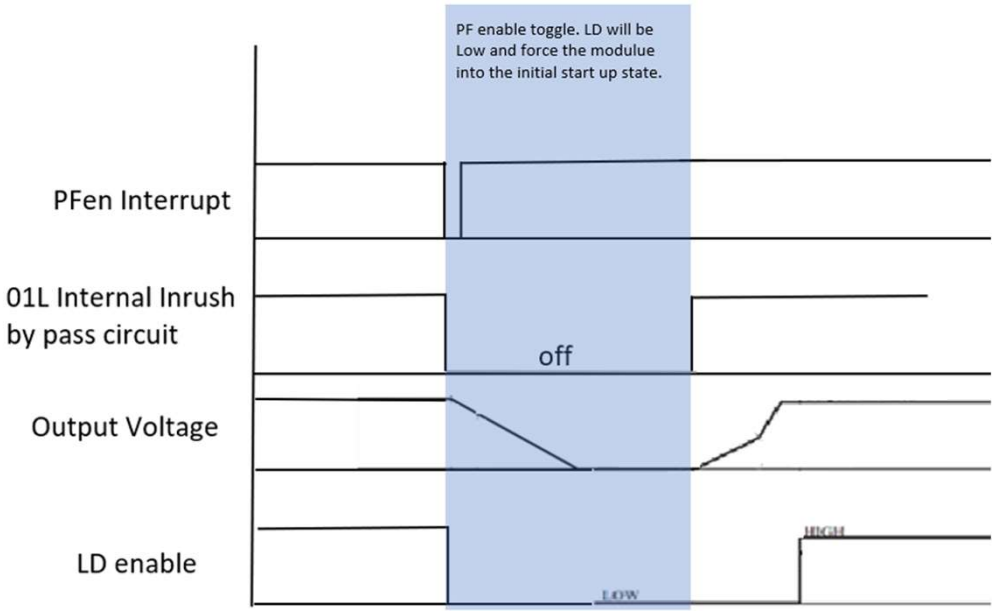


APPLICATION NOTES

Pulse Generator Circuit to Toggle PF enable Circuit



Timing diagram of toggling PF enable pin



APPLICATION NOTES

Brown Out Ride Through

Brown Out condition occurs when there is a transient break in input voltage. During this period the external output bulk capacitor holds up the voltage to the load until input power is restored. When the input voltage is restored the PFC module will continue delivering power to the load.

After a Brown Out condition where the output voltage has not dropped below 292Vdc, the module will recover when input power is restored. The PFW signal can be used to monitor input power loss.

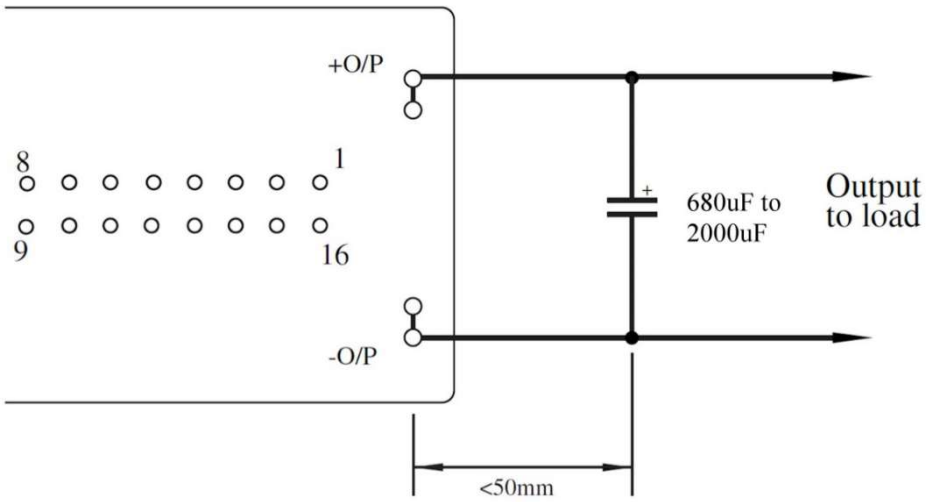
Thermal Data

Natural convection thermal impedance of the AIF06ZPFC series module package without a heatsink is approximately 4°C/W.

A standard horizontal fin heatsink available from AE (part number APA501-80-006) with 37mm fins and 8.8mm pitch, will reduce module thermal impedance to 0.4°C/W with a forced air flow of 2.5m/s (500LFM) when mounted with a thermal pad (AE P/N APA502-80-001) between heatsink and module.

Output Capacitor

The AIF06ZPFC series module requires an output hold-up capacitor of between 680uF and 2000uF to prevent the module from disabling due to fluctuations in output voltage. Ideally the capacitor should be connected directly to the PFC output pins. If this is not possible, the connection is recommended less than 50mm from the output pins.



Selecting an External Output Capacitor

The output capacitor value is determined by the following factors:

1. RMS ripple current.
2. Peak-to-peak output ripple voltage.
3. Hold-up time.
4. Expected lifetime of the capacitor.

APPLICATION NOTES

RMS Ripple Current

The maximum permissible RMS ripple current for the output capacitor should be greater than the RMS ripple current for the application. The ripple current for the PFC module can be approximated as

$$I_{rms} = (P_O / Eff) \times 1/\sqrt{(V_O \times V_{rms})}$$

where :
P_O = output power (W)
Eff = efficiency (%)
V_O = output voltage (V)
Vrms = input rms voltage (V)

This gives the ripple current at 280KHz. The maximum ripple current for capacitors is usually specified at 120Hz. To convert from 280KHz to 120Hz the Irms figure should be divided by 1.4.

Peak to Peak Output Ripple Voltage

The ac input causes a ripple on the output voltage. The size of the ripple is inversely proportional to the size of the capacitor. Therefore the maximum allowable ripple voltage should be decided in order to calculate the size of capacitor required. This may be calculated using the following equation:

$$C_O = P_O / (2\pi f \times Eff \times V_O \times V_{ripple})$$

where :
C_O = output capacitance (F)
Eff = efficiency (%)
f = input voltage frequency (Hz)
V_O = output voltage (V)
V_{ripple} = output ripple voltage (V)

APPLICATION NOTES

Hold-Up Time Requirement

The output capacitor value is different for different hold-up time requirements. The minimum capacitance corresponding to the required hold-up time of a system comprised of AE DC/DC power modules and an AIF06ZPFC series module can be calculated as follows:

$$C_{O,min} = (2 \times P_O \times T_{hold})/[(V_O - V_{ripple})^2 - (V_{min})^2]$$

Where :

$C_{O,min}$ = output capacitance (F)
P_O = output power (W)
T_{hold} = hold up time (sec)
V_O = output voltage (V)
V_{ripple} = output ripple voltage (V)
V_{min} = 290V of LD Enable OFF level (or minimum input voltage for DC/DC module if the setting is higher than 290V)

For example:

An AIF06ZPFC series module drives 3pcs of AE AIF50B300 600W modules @ $12V_O$. Efficiency of the AIF50B300 module is 90%, the minimum input voltage is 290V, the output voltage of the PFC is 400V, the required hold-up time is 20mS and the peak-to-peak voltage V_{ripple} is chosen to be 16V.

$$C_{O,min} = \frac{2 \times (3 \times 600/0.90) \times 0.02}{[(400-16)^2-290^2]} = 1270\mu F$$

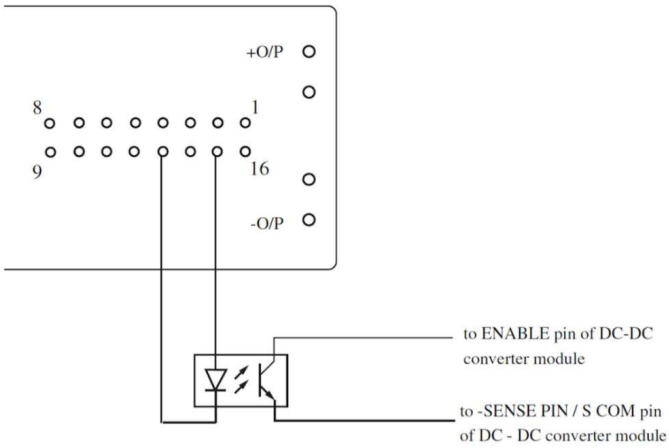
This figure is the minimum capacitance. To allow for capacitor tolerances and aging effects the actual value is recommended more than 1.3 times

APPLICATION NOTES

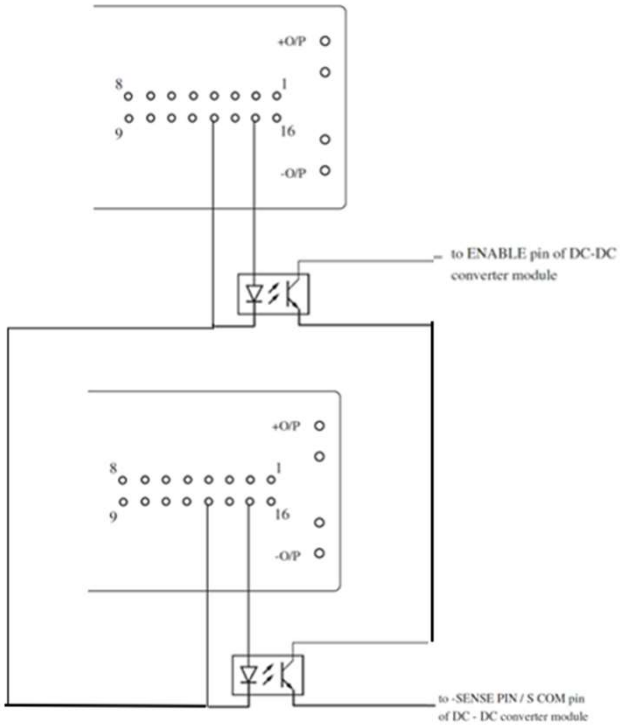
Connections to enable DC-DC converters

The output from the AIF06ZPFC's LD ENABLE (pin 13) can directly drive an opto-coupler to provide an isolated signal to enable the power output of one or more AE DC-DC converter modules.

Single



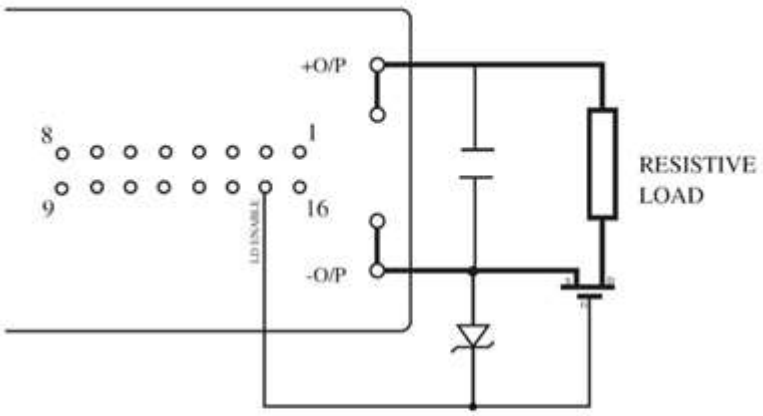
2+0 parallel mode Connection



APPLICATION NOTES

General Connections to Enable a Resistive Load

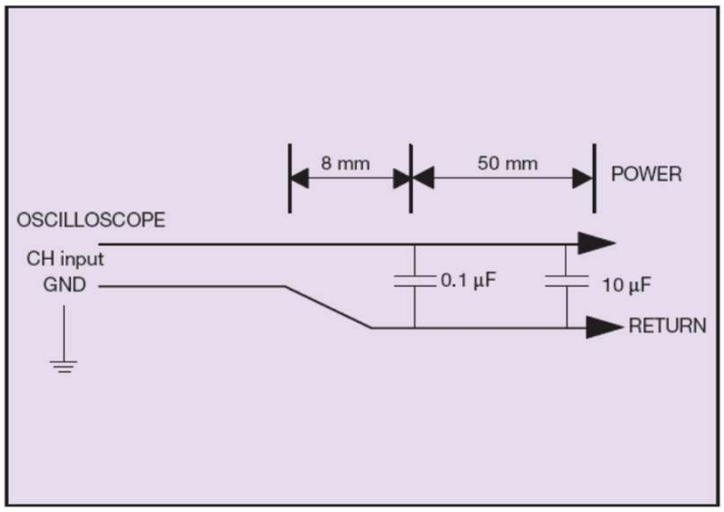
For enabling resistive loads other than AE DC-DC converters the following circuit can be used. The LD ENABLE pin can directly drive a MOSFET with a 15V zener clamping the gate voltage.



APPLICATION NOTES

Output Ripple and Noise Measurement

The setup outlined in the diagram below has been used for output voltage ripple and noise measurements on the AIF06ZPFC series module. When measuring output ripple and noise, a scope jack in parallel with a 0.1uF ceramic chip capacitor, and a 10uF aluminum electrolytic capacitor should be used. Oscilloscope should be set to 20MHz bandwidth for this measurement.

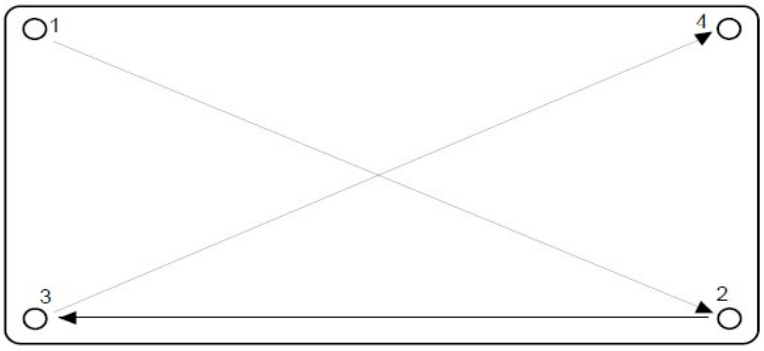


APPLICATION NOTES

Mounting Recommendations

Recommended torque setting and sequence for AIF06ZPFC series module M3 mounting screws.

Screw Size	Torque
M3	4-6kg-cm (3.5-5.2lb-in)



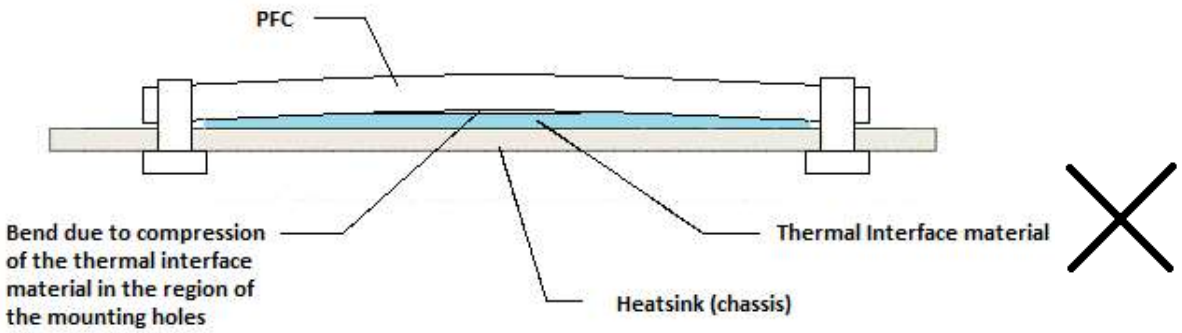
Heatsink Torquing Sequence

Recommended Flatness Spec for PFC Heatsink:

To provide optimal thermal contact between heatsink and module, it is recommended that the mating surface of the heatsink should have a surface flatness of no greater than 0.1mm.

Recommended PFC Thermal Interface Material:

The use of a thermal pad or a thin layer of thermal grease is recommended. If a thermal pad is used, its thickness should be 0.5mm or less, to avoid bending the PFC baseplate due to compression of the interface material in the region of the mounting holes (see below illustration):



APPLICATION NOTES

Soldering

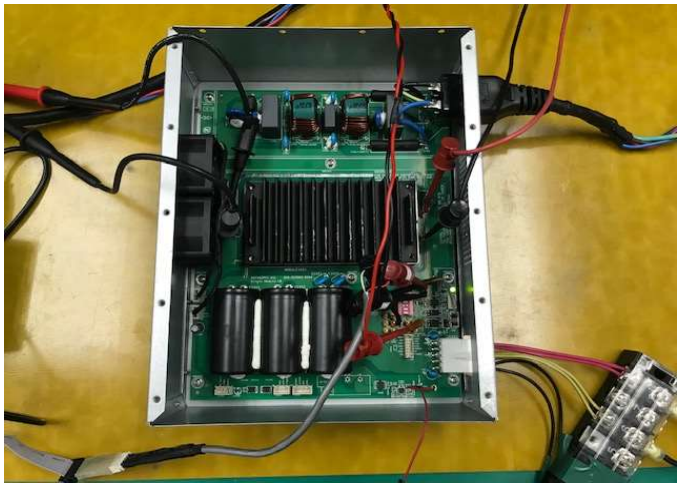
The AIF06ZPFC series module is intended for standard manual or wave soldering.
When wave soldering is used, the temperature on pins is specified to maximum 260^{O}C for maximum 7 sec.
When manual soldering is used, the iron temperature should be maintained at 300^{O}C ~ 380^{O}C and applied to the converter pins for less than 10 sec. Longer exposure can cause internal damage to the converter.
Cleaning solder joint can be performed with cleaning solvent IPA or simulative.
Contact AE for further information.

APPLICATION NOTES

Appendix A

Test condition

$T_{ambient}$: 25°C
V ADJ: Connect to S GND
Output Cap: 680 uF x 2
S GND not connected to PGND in application board
For paralleled operation, short each AIF06ZPC 's S GND together.



RECORD OF REVISION AND CHANGES

Issue	Date	Description	Originators
1.0	09.02.2019	First Issue	K. Wang
1.1	10.08.2019	Add “actual phase shift between each phase”	K. Wang
1.2	12.11.2019	Update PMBus command list	K. Wang
1.3	04.08.2020	1. Add conduct emissions test result (2 Units) 2. Add note for PV_AUX 3. Add circuit & options for parallel application	K. Wang
1.4	05.12.2020	Add component MPN List (single module and two modules)	K. Wang
1.5	07.30.2020	Update OVP, low input voltage and other issues from design	K. Wang
1.6	09.28.2020	Add note for waveform monitoring or measurement New AE Template	K. Wang
1.7	11.19.2020	Update PMBus Clock frequency Update STATUS_BYTE to read only	K. Wang
1.8	12.18.2020	Update 80h each bit description	K. Wang
1.9	02.25.2021	Update per design’s feedback	J. Ma
2.0	03.16.2021	Update template issue per cooperate request Add latest eff curve provided by DE	K. Wang
2.1	03.31.2021	Update PFW ADJ	K. Wang
2.2	10.21.2021	1. Update the number of parallel unit (6 max.) 2. Update the performance curve (Figure 3&4)	J. Ma
2.3	08.28.2023	Add warning for LD ENABLE	K. Wang
2.4	01.16.2024	Add Single Module Enhanced Performance EMI filter	K. Wang
2.5	02.29.2024	Remove PFC Switch Frequency	K. Wang
2.6	06.04.2024	1. Add recommended footprint on page14 2. Block diagram updated on page 26 3. Block diagram updated on page 38 4. Added earth connection method on page 38	K. Tsang.

ABOUT ADVANCED ENERGY

Advanced Energy (AE) has devoted more than three decades to perfecting power for its global customers. AE designs and manufactures highly engineered, precision power conversion, measurement and control solutions for mission-critical applications and processes.

Our products enable customer innovation in complex applications for a wide range of industries including semiconductor equipment, industrial, manufacturing, telecommunications, data center computing, and medical. With deep applications know-how and responsive service and support across the globe, we build collaborative partnerships to meet rapid technological developments, propel growth for our customers, and innovate the future of power.

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