

CSU3200AT SERIES

M-CRPS Power Supply

3200 W Distributed Power System



PRODUCT DESCRIPTION

Advanced Energy's CSU3200AT series power supply is designed to provide a flexible power conversion solution for compute, storage, and networking equipment in the modular hardware common redundant power supply (M-CRPS). The 3200W model is in the standard 1U x 73.5 mm x 185 mm form factor. The series of power supply can cover cost-sensitive entry level systems, or power hungry applications where there are space constraints.

SPECIAL FEATURES

- 3200W output power
- 1U power supply
- Ultra high-density design
- Active power factor correction
- EN61000-3-2 harmonic compliance
- Inrush current control
- 80 PLUS® Titanium efficiency
- N+N, N+1 redundant
- Hot-pluggable
- Active current sharing
- Closed loop throttle
- Cold redundancy
- 2 year warranty
- PMBus™ compliant

SAFETY

- UL/cUL
- CB Test Certificate
- CE Mark
- CQC BSMI
- KC
- EAC
- BIS

COMPLIANCE

- Conducted/Radiated EMI Class A Limits
- RoHS
- IEC 60950/62368

AT A GLANCE

Total Power

180 to 198VAC 2900 W
198 to 264VAC 3200 W
240VDC 3200 W

Input Voltage

180 to 264 VAC
198 to 264 VAC
192 to 310 VDC

Number of Outputs

Main and Standby



TABLE OF CONTENTS

Section 1	Model Numbers	4
Section 2	Electrical Specifications	5
2.1	Absolute Maximum Ratings	5
2.2	Input Specifications	6
2.3	Output Specifications	8
2.4	System Timing Specifications	9
2.5	CSU3200AT-3-3M0 Performance Curves	13
2.6	Protection Function Specifications	15
Section 3	Mechanical Specifications	17
3.1	Mechanical Outlines	17
3.2	Mechanical Data	18
3.3	Unit Packaging Requirement	18
3.4	Connector Definitions	19
3.5	Power/Signal Mating Connectors and Pin Types	20
3.6	Connector Definitions LED Indicator Definition	21
Section 4	Environmental Specifications	22
4.1	EMC Immunity	22
4.2	Safety Certifications	23
4.3	EMI Emissions	24
4.4	Short-Term Excursion Temperature	26
4.5	Forced Air Cooling	26
4.6	Storage and Shipping Temperature	27
4.7	Altitude	27
4.8	Humidity	27
4.9	Vibration	27
4.10	Shock	28

TABLE OF CONTENTS

Section 5	Power and Control Signal Descriptions	29
5.1	AC Input Connector	29
5.2	Output Connector – Power Blades	29
5.3	Output Connector – Control Signals	29
Section 6	Communication BUS Description	36
6.1	I ² C Bus Signals	36
6.2	Logic Levels	38
6.3	Device Addressing	39
6.4	I ² C Clock Synchronization	40
6.5	Cold Redundancy	41
6.6	Black Box	45
6.7	FRU (EEPROM) Data	49
Section 7	PMBus™ Specification	56
7.1	CSU3200 Series PMBus™ General Instructions	56
7.2	Firmware Update Process	66
7.3	PSU Flow during Powering ON	67
Section 8	Firmware Security	68
8.1	MCRPS Product Cyber Security Overview	68
8.2	Algorithms, Certificate, and Key Storage	69
8.3	Runtime Software Attestation	70
Section 9	Application Notes	71
9.1	Current Share	71
9.2	Output Ripple and Noise Measurement	72
Section 10	Record of Revision and Changes	73

SECTION 1 MODEL NUMBERS

Standard	Output Voltage	Minimum Load	Maximum Load	Stand-By Supply	Air Flow Direction
CSU3200AT-3-3M0	12.2 VDC	0A	262.3A	12.0 VDC at 3 A	Forward (DC Connector to Handle)

Options

None

Available Load Board

Model Number	Description
700-029450-0000	Single Unit Load Board
700-029450-0001	Two Units Load Board

Family Comparison

Model Number	Input Type	Output Voltage	Output Power	Standby Output	Efficiency	Dimension
CST1800AT-3-3M0	AC/DC Input	12.2 VDC	1800W	12 VDC at 3 A	Titanium	1U x 60mm x 185mm
CSU2400AT-3-3M0	AC/DC Input	12.2 VDC	2400W	12 VDC at 3 A	Titanium	1U x 73.5mm x 185 mm
CSU3200AT-3-3M0	AC/DC Input (AC High-line only)	12.2 VDC	3200W	12 VDC at 3 A	Titanium	1U x 73.5mm x 185 mm
CSU3200AT-3-6M0	AC/DC Input (AC High-line and Low-line)	12.2 VDC	3200W	12 VDC at 3A	Titanium	1U x 73.5mm x 185 mm
CSU3200ADC-3-3M0	DC/DC Input	12.2 VDC	3200W	12 VDC at 3A	94% peak efficiency	1U x 73.5mm x 185 mm
CSU3600AT-9-3M0	AC/DC Input	54.0 VDC	3600W	12 VDC at 3 A	Titanium	1U x 73.5mm x 185 mm

SECTION 2 ELECTRICAL SPECIFICATIONS

2.1 Absolute Maximum Ratings

Stress in excess of those listed in the “Absolute Maximum Ratings” may cause permanent damage to the power supply. These are stress ratings only and functional operation of the unit is not implied at these or any other conditions above those given in the operational sections of this TRN. Exposure to any absolute maximum rated condition for extended periods may adversely affect the power supply’s reliability.

Table 1. Absolute Maximum Ratings						
Parameter	Models	Symbol	Min	Typ	Max	Unit
Input Voltage	AC continuous operation	$V_{IN,AC}$	180	-	264	VAC
			198	-	264	VAC
	DC continuous operation	$V_{IN,DC}$	192	240	310	VDC
Maximum Output Power ¹	All models	$P_{O,max}$	-	-	3200	W
Isolation Voltage	Input to outputs		-	-	3000	VDC
Normal Operating Temperature	All models	T_A	-5	-	55	°C
Cold Start Temperature	All models	T_{STG}	-5	-	-	°C
Humidity (non-condensing)	Operating		-	-	85	%
	Non-operating		-	-	95	%
Altitude	Operating		-	-	3050	Meters
	Non-operating		-	-	15200	Meters
MTBF ²	All models		400	-	-	KHours
Operating Life ³	80% Load		5	-	-	Years
	50% Load		7	-	-	Years
Fan L10 Life @ 50°C	All models		-	-	43.2	KHours

Note 1 - Output power is 2900W at 180 to 198VAC

Note 2 - MTBF prediction shall be completed in accordance with Telcordia SR-332, Method 1 Case 3, 40°C

Note 3 - It is calculated under 55°C ambient temperature, 220 to 240 Vac input.

SECTION 2 ELECTRICAL SPECIFICATIONS

2.2 Input Specifications

Table 2. Input Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Operating Input Voltage, AC	All	$V_{IN,AC}$	180 198	- -	264 264	VAC VAC
Operating Input Voltage, DC	All	$V_{IN,DC}$	192	240	310	VDC
Input AC Frequency	All	$f_{IN,AC}$	47	50/60	63	Hz
Maximum Input Current	$V_{IN,AC} = 180VAC$ at 2900W $V_{IN,AC} = 200VAC$ at 2900W $V_{IN,AC} = 198VAC$ at 3200W $V_{IN,AC} = 240VAC$ at 3200W $V_{IN,AC} = 264VAC$ at 3200W $V_{IN,DC} = 192VDC$ $V_{IN,DC} = 240VDC$	$I_{IN,max}$	- - - - - - -	- - - - - - -	18 16 18 15 14 18.2 14.5	A A A A A A A
No Load Input Current ($V_O = On$, $I_O = 0A$, $I_{SB} = 0A$)	$V_{IN,AC} = 180 VAC$	$I_{IN,no-load}$	-	-	200	mA
No Load Input Power ($V_O = On$, $I_O = 0A$, $I_{SB} = 0A$)	$V_{IN,AC} = 180 VAC$	$P_{IN,no-load}$	-	-	8.5	W
Standby Input Current ($V_O = Off$, $I_{SB} = 0A$)	$V_{IN,AC} = 180 VAC$	$I_{IN,Standby}$	-	-	200	mA
Standby Input Power ($V_O = Off$, $I_{SB} = 0A$)	$V_{IN,AC} = 180 VAC$	$P_{IN,Standby}$	-	-	4	W
Input iTHD	$V_{IN,AC} = 240 VAC$ $I_O \geq 0\%I_{O,max}$ $I_O \geq 5\%I_{O,max}$ $I_O \geq 10\%I_{O,max}$ $I_O \geq 20\%I_{O,max}$ $I_O \geq 50\%I_{O,max}$ $I_O \geq 100\%I_{O,max}$	iTHD	- - - - - -	- - - - - -	40 25 10 7.5 5 4	%
Harmonic Line Currents	All	THD	Per IEC61000-3-2			
Power Factor	$I_O = 10\%I_{O,max}$ $I_O = 20\%I_{O,max}$ $I_O = 50\%I_{O,max}$ $I_O = 100\%I_{O,max}$	PF	0.92 0.96 0.98 0.99	- - - -	- - - -	
Startup Surge Current (Inrush) ¹		$I_{IN,surge}$	-	-	35	Apk
Turn-on Voltage Recommended 5V hysteresis	AC High Line	$V_{IN,AC}$	174	-	-	VAC
	AC Low Line	$V_{IN,AC}$	-	-	-	VAC
	DC Input	$V_{IN,DC}$	180	-	-	VDC
Turn-off Voltage Recommended 5V hysteresis	AC High Line	$V_{IN,AC}$	169	-	-	VAC
	AC Low Line	$V_{IN,AC}$	-	-	-	VAC
	DC Input	$V_{IN,DC}$	175	-	-	VDC

Note 1 - AC line inrush current shall not exceed 35A peak ignoring the initial 500us of the EMI filter charge, for up to one-half of the AC cycle, after which the power supply is allowed to have a secondary inrush event for up to PSU model label current rating Amperes and lasting for up to 2500ms, the input current should be no more than the specified maximum input current. The peak inrush current shall be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

SECTION 2 ELECTRICAL SPECIFICATIONS

2.2 Input Specifications

Table 2. Input Specifications						
Parameter	Condition	Symbol	Min	Typ	Max	Unit
Leakage Current to Earth Ground ¹			-	-	0.583	mA
Operating Efficiency	$V_{IN,AC} = 180 \text{ VAC}$	η	92	-	-	%
	$V_{IN,AC} = 198 \text{ VAC}$		92	-	-	%
	$V_{IN,AC} = 200 \text{ VAC}$		92.5	-	-	%
	$V_{IN,AC} = 220 \text{ VAC}$		92.5	-	-	%
	$V_{IN,AC} = 240 \text{ VAC}$		92.5	-	-	%
	$V_{IN,AC} = 264 \text{ VAC}$		92.5	-	-	%
	$V_{IN,DC} = 192 \text{ VDC}$		92	-	-	%
	$V_{IN,DC} = 240 \text{ VDC}$		92.5	-	-	%
Hold-up Time	$V_{IN,DC} = 310 \text{ VDC}$		93	-	-	%
			11	-	-	ms

Note 1 – Leakage current is based upon 6 power supplies in parallel, to meet 3.5mA limit at platform level.

SECTION 2 ELECTRICAL SPECIFICATIONS

2.3 Output Specifications

Table 3. Output Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Factory Set Voltage	$V_{IN,AC} = 230VAC$ $I_O = 50\%I_{O,max}$ $T_A = 25^{\circ}C$	V_O	12.17	12.20	12.23	VDC
	$V_{IN,AC} = 230VAC$ $I_{SB} = 50\%I_{SB,max}$ $T_A = 25^{\circ}C$	V_{SB}	12.045	12.075	12.105	VDC
Line and Load Regulation	0% to 100% $I_{O,max}$	V_O	12.06	-	12.34	VDC
Dynamic Loading	60% load change starting anywhere from 1A to 40% load, slew rate 2.5A/us	V_O	11.16	-	12.84	VDC
	1A load change starting anywhere from 0% to 50% load, slew rate 0.5A/us	V_{SB}	11.04	-	12.96	VDC
Output Ripple, pk-pk	Measured at the output mating connector with a 10uF/16V Low ESR capacitor and a 0.1uF ceramic capacitor and at 20MHz bandwidth	V_O	-	-	120	mV _{PK-PK}
		V_{SB}	-	-	120	mV _{PK-PK}
Output Current ^{1,2}	All	I_O	0	-	262.3	A
	All	I_{SB}	0	-	3	A
Main Output Current Share Error (CSE)	5% to 100% $I_{O,max}$	$\pm \%I_{O,max}$	-	-	4	%
Number of Parallel Units	Main output current share connected		-	-	6	Units
Load Capacitance	Main Output	C_O	3,300	-	70,000	uF
	Standby		270	-	4700	uF
	External Capacitance		-	-	2,000	uF

Note 1 - The absolute maximum peak current should not exceed 100% $I_{O,max}$ during the test.

Note 2 - Permissible overload of up to 283A under short-term conditions. See over-current protection section.

SECTION 2 ELECTRICAL SPECIFICATIONS

2.4 System Timing Specifications

Table 4. System Timing Specifications

Label	Parameter	Min	Typ	Max	Unit
T_{vout_rise}	Output voltage rise time for 12V and 12V _{SB} from 10% to within regulation limits.	10	-	70	ms
$T_{off_latch}^1$	This is the time the power supply unit must stay off when being powered off with loss of input. Both outputs must meet this off time: 1) whenever P _{WOK} is de-asserted for the 12V _{main} output; 2) whenever the 12V _{SB} output drops below regulation limits.	500	-	1000	ms
$T_{sb_on_delay}$	Delay from input being applied to 12V _{SB} being within regulation.	-	-	1500	ms
$T_{ac_on_delay}$	Delay from input being applied to all output voltages being within regulation.	-	-	3000	ms
T_{vout_holdup}	Time 12V output voltage stays within regulation after loss of input.	11	-	-	ms
$T_{pwok_holdup}^2$	Delay from input loss to de-assertion of PWOK	5	10	-	ms
$T_{pson_off_delay}$	Delay from PSON# de-asserted to power supply turning off	-	-	5	ms
$T_{pson_on_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	-	400	ms
T_{pson_pwok}	Delay from PSON# deactivate to P _{WOK} being de-asserted.	-	-	3	ms
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	380	-	420	ms
$T_{pwok_off}^2$	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1	-	6 ⁴	ms
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using input or the PSON# signal.	100	-	-	ms
T_{SB_vout}	Delay from 12V _{SB} being in regulation to outputs being in regulation at input turn on.	50	-	1000	ms
T_{12VSB_holdup}	Time the 12V _{SB} output voltage stays within regulation after loss of input.	70	-	-	ms
$T_{vinok_on}^3$	Delay from 12V _{SB} within regulation limits to assertion of VINOK	0	-	50	ms
$T_{vinok_off}^3$	Time from loss of input to de-assertion of VINOK	1000	-	4000	ms

Note 1 - T_{off_latch} flow diagram is shown in [T_{off_latch} Flow Diagram](#).

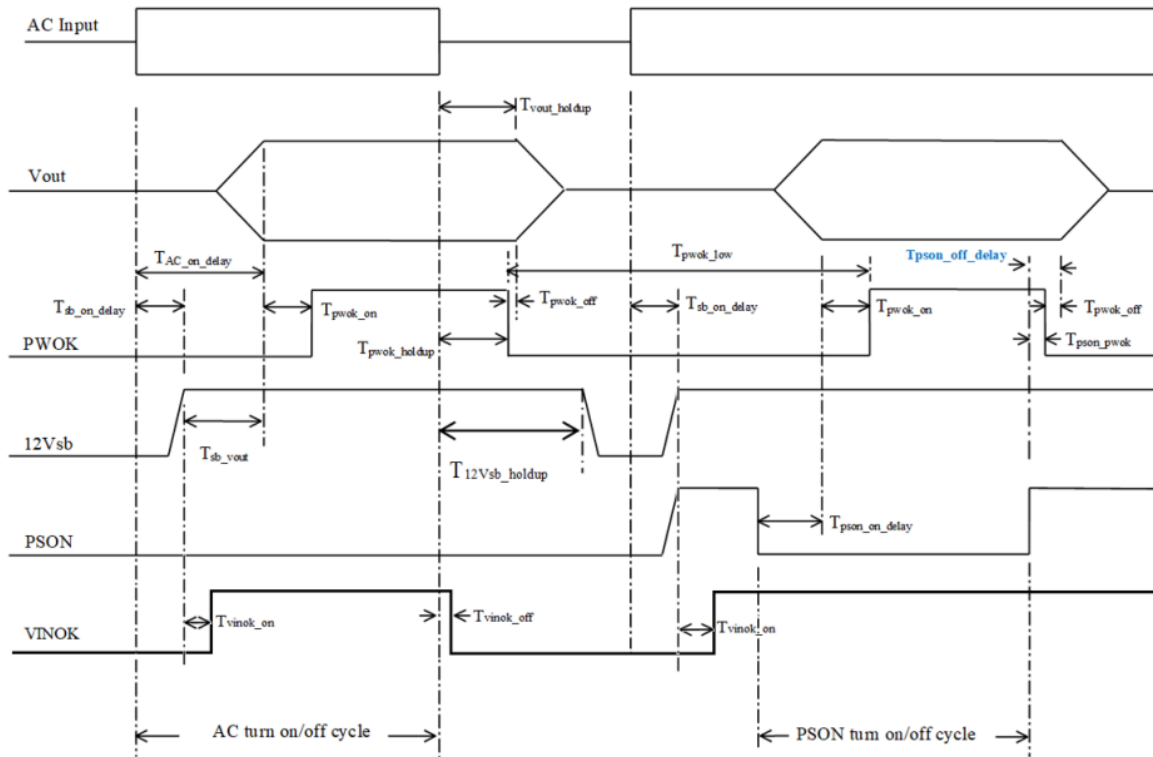
Note 2 - The T_{pwok_holdup} = 1ms and T_{pwok_off} = 10ms, are the default values in the power supply unit when it's being energized, however the system now can configure the warning time established by T_{pwok_off} to have a different value please refer to PWOK Signal Timing Requirements.

Note 3 - Additional logic dependencies are described in [V_{inok} Assertion Logic](#).

Note 4 - T_{pwok_off} can be configure from 1ms (default) to a maximum of 6ms, refer to [PWOK Signal Timing Requirements](#) for more details.

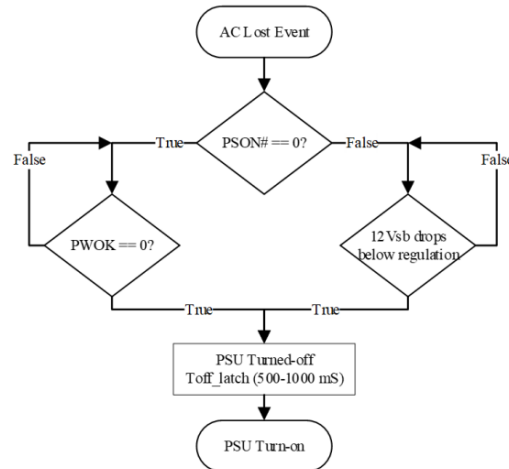
SECTION 2 ELECTRICAL SPECIFICATIONS

2.4 System Timing Diagram



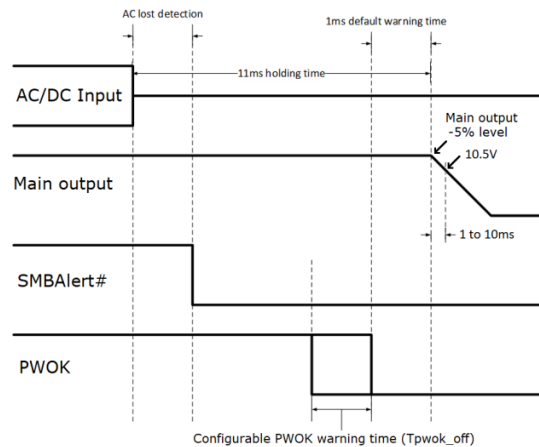
SECTION 2 ELECTRICAL SPECIFICATIONS

$T_{\text{off_latch}}$ Flow Diagram



PWOK Signal Timing Requirements

Timing requirements when the power supply is being energized (AC/DC is applied), however the warning time established by $T_{\text{pwok_off}}$ shall be configurable via PMBus command MFR_PWOK_WARNING_TIME (F0h) using linear format it is recommended to use 1ms steps and the power supply shall guarantee at least the minimum warning time configured, it is recommended to have a jitter no more than 1.5ms. Below shows the timing diagram. $T_{\text{pwok_off}}$ value shall return to default after an AC/DC input cycle only. The figure below shows the timing diagram. $T_{\text{pwok_off}}$ value shall return to default after an AC/DC input cycle only with a complete power supply power off (indicator LED off and secondary side MCU de-energized)



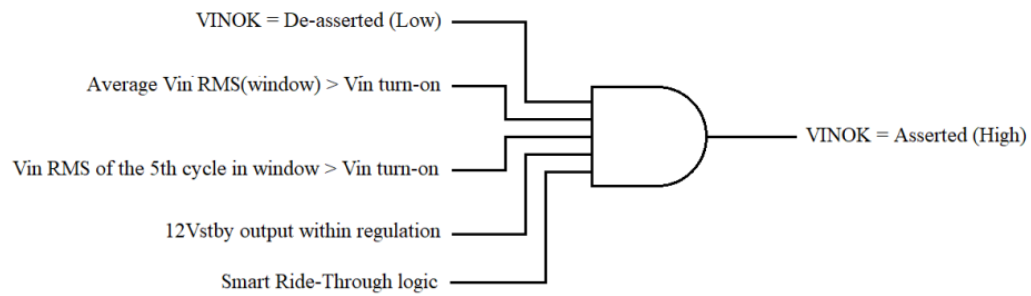
The main output shall have a slope decay of 1-10ms from 11.40V to 10.5V when going down using a 5% loading condition and the maximum capacitance across the main output as defined in the below capacitive loading conditions:

Output	Min	Max	Unit
12V Main output	2,000 ¹	70,000	uF
12V Standby output	270	4,700	uF

Note 1 - The minimum capacitive load on this output is required to hold regulation during Cold Redundancy mode PSU failures and PSU hot swapping.

SECTION 2 ELECTRICAL SPECIFICATIONS

V_{inok} Assertion Logic



SECTION 2 ELECTRICAL SPECIFICATIONS

2.5 CSU3200AT-3-3M0 Performance Curves



Figure 1: CSU3200AT-3-3M0 Turn-On Delay via AC Mains

$V_{in} = 240V_{ac}$ Load: $I_O = 262.3A$ $I_{SB} = 3A$

Ch 1: AC Mains Ch 2: V_O Ch 3: V_{SB} Ch 4: PWOK



Figure 2: CSU3200AT-3-3M0 Turn-On Delay via PSON

$V_{in} = 240V_{ac}$ Load: $I_O = 262.3A$ $I_{SB} = 3A$

Ch 1: AC Mains Ch 2: V_O Ch 3: PSON Ch 4: PWOK

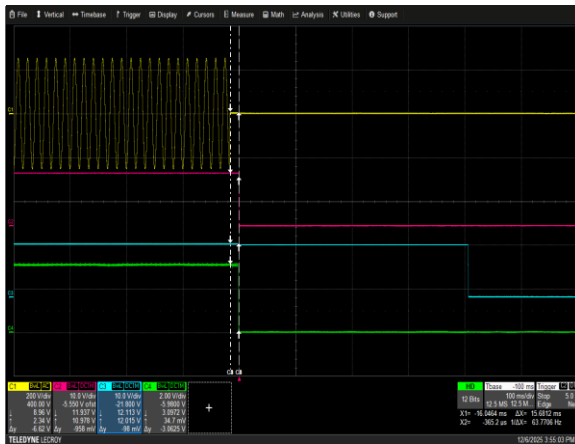


Figure 3: CSU3200AT-3-3M0 Hold-Up Time

$V_{in} = 180V_{ac}$ Load: $I_O = 262.3A$ $I_{SB} = 3A$

Ch 1: AC Mains Ch 2: V_O Ch 3: V_{SB} Ch 4: PWOK

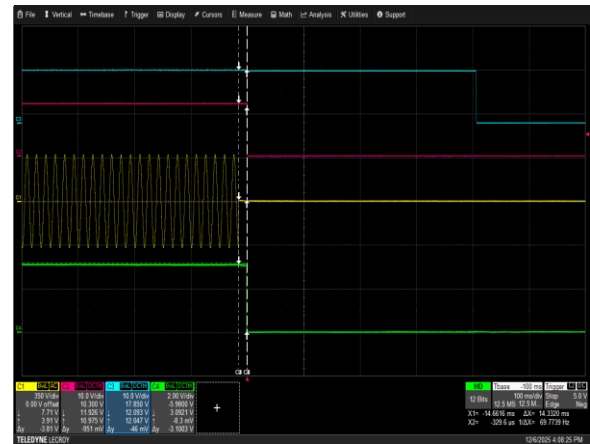


Figure 4: CSU3200AT-3-3M0 Hold-Up Time

$V_{in} = 264V_{ac}$ Load: $I_O = 262.3A$ $I_{SB} = 3A$

Ch 1: AC Mains Ch 2: V_O Ch 3: V_{SB} Ch 4: PWOK



Figure 5: CSU3200AT-3-3M0 VIN_GOOD Assert Characteristic

$V_{in} = 240V_{ac}$ Load: $I_O = 262.3A$ $I_{SB} = 3A$

Ch 1: AC Mains Ch 2: V_O Ch 3: VIN_GOOD Ch 4: PWOK

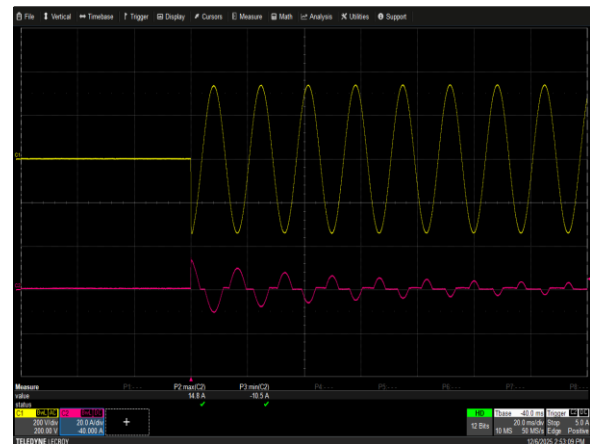


Figure 6: CSU3200AT-3-3M0 VIN_GOOD Inrush Current

$V_{in} = 240V_{ac}$ Load: $I_O = 0A$

Ch 1: AC Mains Ch 2: V_O

SECTION 2 ELECTRICAL SPECIFICATIONS

2.5 CSU3200AT-3-3M0 Performance Curves



Figure 7: CSU3200AT-3-3M0 Output Voltage Startup Characteristic
 $V_{in} = 240V_{ac}$ Load: $I_o = 262.3A$ $I_{SB} = 3A$
 Ch 1: V_O

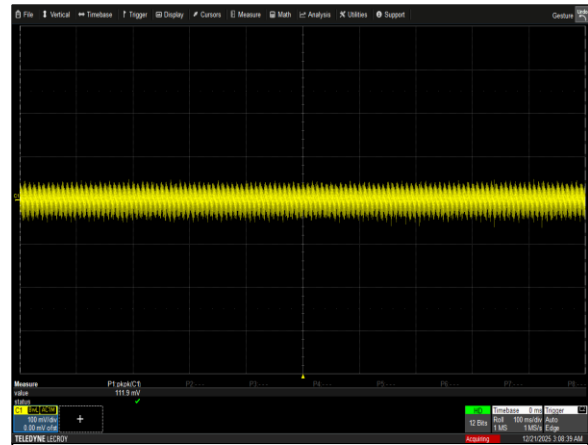


Figure 8: CSU3200AT-3-3M0 Ripple and Noise Measurement
 $V_{in} = 240V_{ac}$ Load: $I_o = 263.3A$ $I_{SB} = 3A$
 Ch 1: V_O



Figure 9: CSU3200AT-3-3M0 Turn Off Characteristic via PSOn
 Load: $I_o = 262.3A$ $I_{SB} = 3A$
 Ch 2: V_O Ch 3: PSOn Ch 4: PWOK

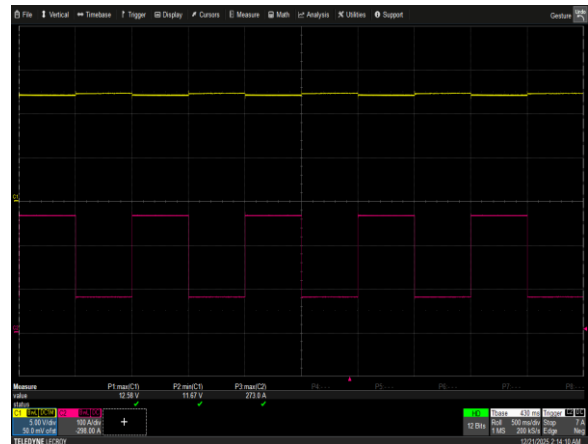


Figure 10: CSU3200AT-3-3M0 Transient Response - V_O Deviation
 30% to 100% load change 2.5A/uS slew rate $V_{in} = 240V_{ac}$
 Ch 1: V_O Ch 2: I_o

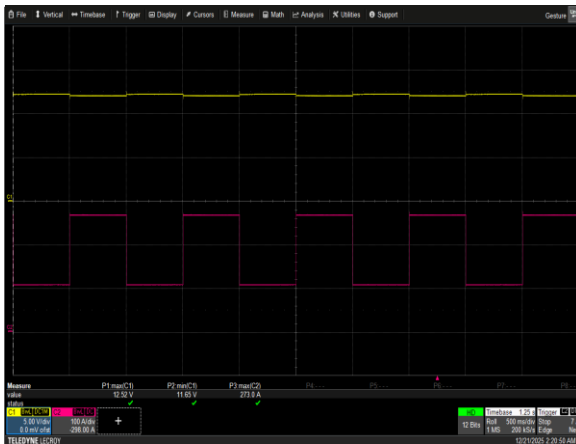


Figure 11: CSU3200AT-3-3M0 Transient Response - V_O Deviation
 100% to 40% load change 2.5A/uS slew rate $V_{in} = 240V_{ac}$
 Ch 1: V_O Ch 2: I_o

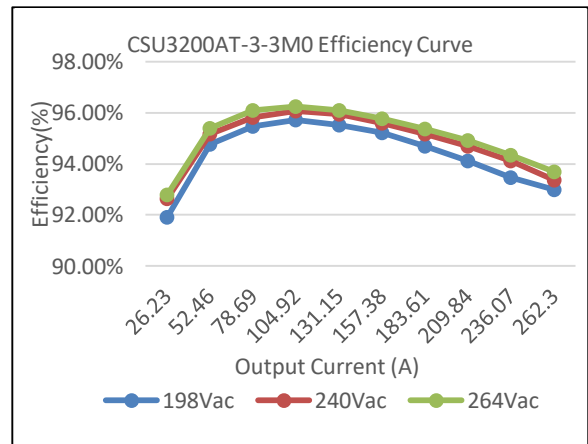


Figure 12: CSU3200AT-3-3M0 Efficiency Curve @ 25°C
 Loading: $I_{o_main} = 10\%$ increment to I_{o_max}

SECTION 2 ELECTRICAL SPECIFICATIONS

2.6 Protection Function Specifications

Input Fuse

CSU3200AT series power supply is equipped with an internal non-user serviceable 20A, rated voltage at 420Vac, 420Vdc fuse to UL248-14 for fault protection on L line input.

Over Voltage Protection (OVP)

When the OVP circuit is activated (main output and standby), the power supply must latch off requiring PSON or the input power to be recycled manually to reset the power supply after the fault has been removed.

A failure on the reference used for regulating the output voltage should not cause the power supply to lose its ability to protect against over-voltage.

Parameter	Min	Nom	Max	Unit
Main Output Overvoltage	14	-	15	V
Standby Output Overvoltage	14	-	15	V

Short Circuit Protection (SCP)

A short circuit, which is defined as an impedance of 10 mohms or less, applied to any output during start-up or while running will not cause any damage to the power supply (connectors, components, PCB traces, etc.).

When the standby output is shorted, the output may go into “hiccup mode.” When the standby output attempts to restart, the maximum peak current from the output must be less than 10A. The maximum average current, taking into account the “hiccup” duty cycle, must not exceed rated dc output current of the standby.

Over Temperature Protection (OTP)

The power supply is internally protected against over temperature conditions. When the OTP limit is reached, all outputs except standby, will shutdown and remain off until the over temperature condition no longer exists.

A suitable hysteresis point between the OTP threshold and the recovery point shall be set to ensure there is no frequent on-off cycling of the outputs. The temperature recovery point shall be set well-within the operating temperature range. Upon reaching the temperature recovery point, all outputs shall autorecover.

In an OTP condition, the power supply will shut down. OTW SMBAlert# assertion must always precede the OTP shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to the temperature recovery condition. The OTP trip temperature level shall be at least 4°C higher than the OTW threshold level.

Model Number	Parameter (Inlet Air Temperature)	Min	Max	Unit
CSU3200AT-3-3M0	Over Temperature Warning (OTW)	60		°C
	Over Temperature Shutdown (OTP)	65		°C

SECTION 2 ELECTRICAL SPECIFICATIONS

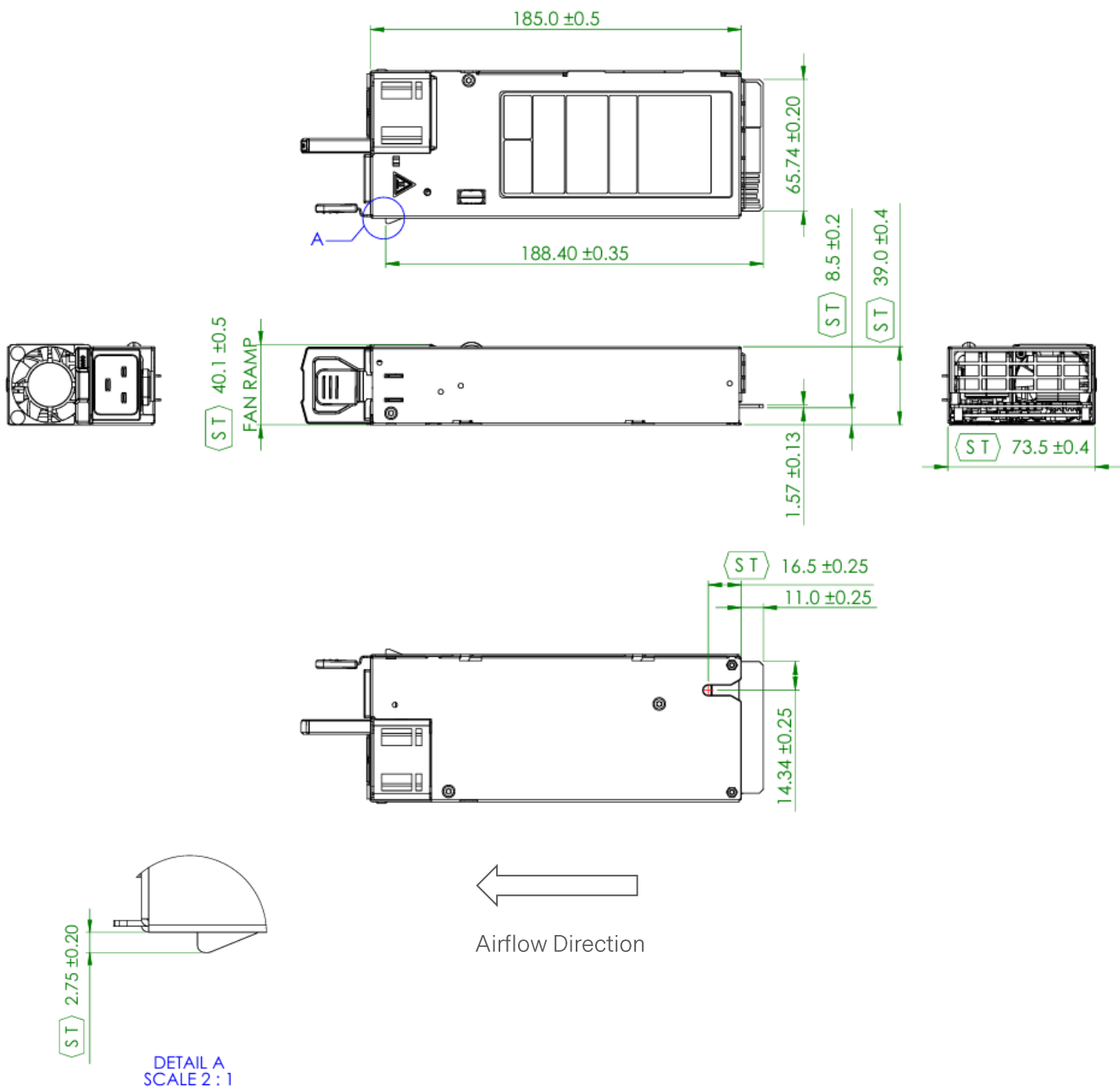
Over Current Protection (OCP)

CSU3200AT series includes internal current limit circuitry to prevent damage in the event of overload or short circuit. It has over current protection (OCP), over current warning (OCW), and over power protection (OPP) limits as defined in table below. They are defined to protect the PSU and to allow peak current to power the system without the PSU shutting down. Fast OCW and slow OCW levels are defined to assert SMBAlert to allow the system to throttle power to protect the PSU and also to allow peak current draws by the system. When OCP trips, it will shutdown and latch off the PSU. The latched PSU is cleared by an AC power cycle or PSON recycle. The power supply can not be damaged from repeated power cycling in this condition. $12V_{SB}$ is auto-recovered after removing OCP limit.

Parameter	Thresholds		Timing		Protection Mode
	Min	Max	Min	Max	
V_O Output Slow Overcurrent Warning	334 ms	-	250 ms	-	SMBAlert
V_O Output Slow Overcurrent Protection	-	-	-	-	Shut down and latch only after min - max timing
V_O Output Fast Overcurrent Warning	373 ms	-	10 ms	-	SMBAlert
V_O Output Fast Overcurrent Protection	373 ms	-	25 ms	-	Foldback then latch after min timing
V_{SB} Output Overcurrent Protection	3.65 ms	-	100 ms	-	Shut down and hiccup mode

SECTION 3 MECHANICAL SPECIFICATIONS

3.1 Mechanical Outlines (unit: mm)



SECTION 3 MECHANICAL SPECIFICATIONS

3.2 Mechanical Data

Table 5. Mechanical Data	
Dimensions (L x W x D)	7.28" x 2.89" x 1U (185mm x 73.5mm x 41mm)
Weight	1.06kg
Cooling	Built in fan

3.3 Unit Packaging Requirement

Packing Dimensions(L x W x D)	Product: 220mm x 78mm x 40mm Carton: 345mm x 298mm x 236mm Pallet: 1220mm x 1016mm x 870mm
Packing Quantities	5 Units / Tray 10 Units / Carton 10 Carton / Layer 30 Carton / Pallet 300 Units / Pallet
Packaging Weight	1.06 kg / Unit 9.8 kg / Carton 315 kg/ Pallet

SECTION 3 MECHANICAL SPECIFICATIONS

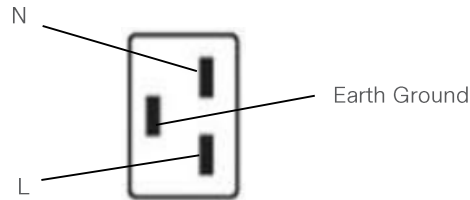
3.4 Connector Definitions

AC Input Connector

Line

Neutral

Earth Ground



Output Connector - Power Blades

A1-A9 (P1-P3) – Main Output Return

A10-A18 (P4-P6) – Main Output (V_O)

B1-B9 (P1-P3) – Main Output Return

B10-B18 (P10-P12) – Main Output (V_O)

Output Connector - Control Signals

A19 (S1) – SDA

A20 (S2) – SCL

A21 (S3) – PS_ON#

A22 (S4) – SMBAlert#

A23 (S5) – PS_Kill

A24 (S6) – N/A

A25 (S7) – PWOK

B19 (S8) – A0

B20 (S9) – A1

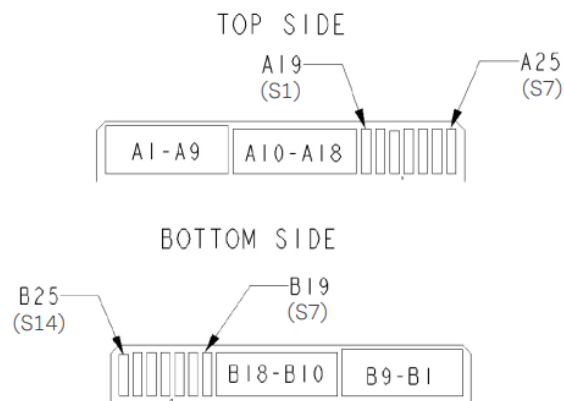
B21 (S10) – 12V_{SB}

B22 (S11) – CR_BUS

B23 (S12) – IShare

B24 (S13) – IMON

B25 (S14) – VINOK



View from power supply output connector end

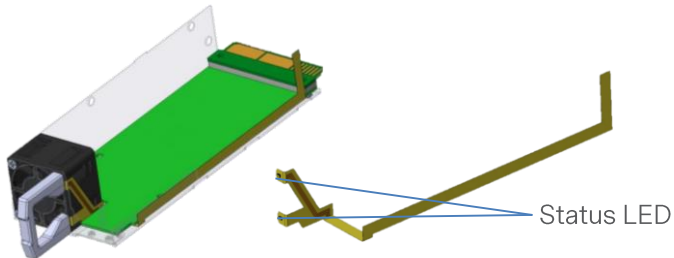
SECTION 3 MECHANICAL SPECIFICATIONS

3.5 Power / Signal Mating Connectors and Pin Types

Table 6. Mating Connectors for CSU3200AT-3-3M0		
Reference	On Power Supply	Mating Connector or Equivalent
AC Input Connector	IEC320-C20	IEC320-C19
Output Connector	Card-edge	FCI Amphenol 10147875-001LF

SECTION 3 MECHANICAL SPECIFICATIONS

3.6 LED Indicator Definitions



One bi-color (green/amber) LED at the power supply front provides the status signal. The status LED conditions are shown on the following table.

Conditions	LED Status
AC present, main output ON, standby output ON	Solid Green
Main output OFF, standby output ON	Solid Green
AC input under voltage, main output OFF, standby output OFF	OFF
Any kind of warning (over current/over temperature/over voltage/fan)	Solid Green
Cold redundant enabled	Solid Green
Any kind of fault (output over voltage/over current/over temperature/ output under voltage, standby output voltage/standby output under voltage)	Amber PWM (2s ON; 1s OFF)
Fan Fault	Amber PWM (2s ON; 1s OFF)
Firmware upgrade	Blinking Green at 4 Hz

SECTION 4 ENVIRONMENTAL SPECIFICATIONS

4.1 EMC Immunity

CSU3200AT series power supply is designed to meet the following EMC immunity specifications.

Table 7. Environmental Specifications			
Test Items	Standard	Test Level	Criteria ¹
Conducted Emissions	EN 55032:2017/A11:2020	Class A. 150k to 30MHz	6dB Margin, average
Radiated Emissions	EN 55032:2017/A11:2020	Class A. 30M to 1GHz	6dB Margin, average
Harmonic Current Emissions	EN 61000-3-2	-	-
Voltage Fluctuations	IEC 61000-3-3	-	-
Electro Static Discharge (ESD) Immunity	EN/IEC 61000-4-2	8kV contact, 15kV air	A
Radiated RF EM Fields Susceptibility	EN/IEC 61000-4-3	10V/m	A
Electrical Fast Transients (EFT) / Bursts	EN/IEC 61000-4-4	+/-2kV	A
Surges - Line to Line (DM) and Line to GND (CM)	EN/IEC 61000-4-5	2kV DM, 3kV CM 2.5kV DM (design margin) 3.5kV CM (design margin)	A
Conducted Immunity	EN/IEC 61000-4-6	10Vrms 0.15MHz – 10MHz 3vrms 10MHz – 30MHz 3V to 1V 30MHz – 80MHz 1V	A
Voltage Dips & Sags	EN 61000-4-11	>95% for 10ms ≤30% for 500ms >95% for 500ms	A A C
Power Frequency Magnetic Field	IEC 61000-4-8	1A/m	A

Note 1 - Performance criteria are based on EN55032. According to the standards, performance criteria are defined as following:

- A - Normal performance during and after the test
- B - Temporary degradation, self-recoverable
- C - Temporary degradation, operator intervention required to recover the operation
- D - Permanent damage

SECTION 4 ENVIRONMENTAL SPECIFICATIONS

4.2 Safety Certifications

The CSU3200AT series power supply is intended for inclusion in other equipment and the installer must ensure that it is in compliance with all the requirements of the end application. This product is only for inclusion by professional installers within other equipment and must not be operated as a stand alone product.

Table 8. Safety Certifications for CSU3200AT Series Power Supply		
Standard	Agency	Description
IEC 60950, IEC 62368, UL/cUL	CE	European Requirements
UL62368-1:2018, CSA 62368-1	UL + CUL	US and Canada Requirements
CB Certificate		All CENELEC Countries
CQC Approval		China Requirements
KC		Korea Certification
EAC		Russia Requirements
BIS		India Requirements
BSMI		Taiwan Requirements
CE Mark		ROHS

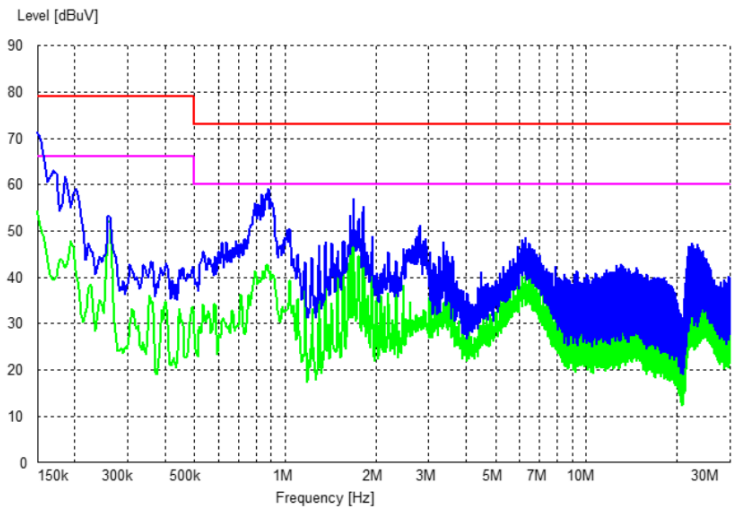
SECTION 4 ENVIRONMENTAL SPECIFICATIONS

4.3 EMI Emissions

The CSU3200AT Seriespower supply has been designed to comply with the Class A limits of EMI requirements of FCC CFR 47 Part 15 Subpart B and EN55032 for emissions and relevant sections of EN55032: 2011 for immunity. The unit is tested at 3200W using resistive load with cooling fan.

Conducted Emissions

The applicable standard for conducted emissions is EN55032 (FCC Part 15). Conducted noise can appear as both differential mode and common mode noise currents. Differential mode noise is measured between the two input lines, with the major components occurring at the supply fundamental switching frequency and its harmonics. Common mode noise, a contributor to both radiated emissions and input conducted emissions, is measured between the input lines and system ground and can be broadband in nature.



The CSU3200AT Seriespower supply has internal EMI filters to ensure the convertor’s conducted EMI levels comply with EN55032 (FCC Part 15) Class A limits. The EMI measurements are performed with resistive loads at maximum rated loading.

Sample of EN55032 conducted EMI measurement at 230Vac input.

Note: Red Line refers to Advanced Energy’s Quasi Peak margin, which is 6dB below the CISPR international limit.
Pink Line refers to Advanced Energy’s Average margin, which is 6dB below the CISPR international limit.

Conducted EMI emissions specifications of the CSU3200AT Series power supply:

Parameter	Model	Symbol	Min	Typ	Max	Unit
FCC Part 15, class A	All	Margin	-	6	-	dB
CISPR 32 (EN55032), class A	All	Margin	-	6	-	dB

SECTION 4 ENVIRONMENTAL SPECIFICATIONS

Radiated Emissions

Unlike conducted EMI, radiated EMI performance in a system environment may differ drastically from that in a stand-alone power supply. The shielding effect provided by the system enclosure may bring the EMI level from Class A to Class B. It is thus recommended that radiated EMI be evaluated in a system environment. The applicable standard is EN55032 Class A (FCC Part 15). Testing AC-DC converters as a stand-alone component to the exact requirements of EN55032 can be difficult because the standard calls for 1m lead to be attached to the input and outputs and aligned such as to maximize the disturbance. In such a set-up, it is possible to form a perfect dipole antenna that very few AC-DC converters could pass. However, the standard also states that an attempt will be made to maximize the disturbance consistent with the typical application by varying the configuration of the test sample.

SECTION 4 ENVIRONMENTAL SPECIFICATIONS

4.4 Short-Term Excursion Temperature

The CSU3200AT series Short-Term Excursion Temperature is shown in the table below.

Table 9. Power supply thermal test conditions					
Model	Output Power	Altitude	Maximum Inlet Temperature	Maximum Exhaust Temperature	Maximum Touch Surface Temperature
CSU3200AT-3-3M0 ¹	3200W	950m	55°C	75°C ²	75°C

Note 1 – Power supply meets Tier 2 level. The temperature limit for the components will be based on their maximum Tj -10°C for components like power semiconductors, magnetics, bulk capacitors, aluminum polymer capacitors at the output of the power supply and PCB.

Note 2 – Power supply will need to have a mylar coating in all the metal parts in the rear part of the chassis when the temperature exceeds 70°C and up to 90°C

4.5 Forced Air Cooling

The CSU3200AT series includes internal cooling fans as part of the power supply assembly to provide forced air-cooling to maintain and control the temperature of devices and ambient temperature in the power supply to appropriate levels. The standard direction of airflow is from the DC connector end to the AC connector end of the power supply.

SECTION 4 ENVIRONMENTAL SPECIFICATIONS

4.6 Storage and Shipping Temperature

The CSU3200AT series power supply can be stored or shipped at temperatures between -40°C to $+70^{\circ}\text{C}$ and relative humidity from 5% to 95% non-condensing.

4.7 Altitude

The CSU3200AT series power supply is certified for safety spacing requires for 3,050 meters altitude. The power supply will not be damaged when stored at altitudes of up to 15,200 meters above sea level.

4.8 Humidity

The CSU3200AT series power supply can operate within specifications when subjected to a relative humidity up to 85% non-condensing. The power supply can be stored in relative humidity up to 95% non-condensing.

4.9 Vibration

The CSU3200AT series power supply shall be performed per power supply vibration test procedure:

Non-operating random vibration

Acceleration	2.2		gRMS
Frequency Range	5 - 500		Hz
Duration	15		Mins
Direction	All 6 sides tested		
PSD Profile	FREQ (Hz)	SLOPE (db/oct)	PSD (g²/Hz)
	5	/	0.01
	20	/	0.01
	500	/	0.01

Operating random vibration

Acceleration	0.5		gRMS
Frequency Range	7 - 800		Hz
Duration	30		Mins
Direction	All 6 sides except AC connection		
PSD Profile	FREQ (Hz)	SLOPE (db/oct)	PSD (g²/Hz)
	7	/	0.00015
	20	/	0.014
	140	/	0.014
	312	/	0.000065
	400	/	0.000035
	600	/	0.000035
	800	/	0.000023

SECTION 4 ENVIRONMENTAL SPECIFICATIONS

4.10 Shock

The CSU3200AT series power supply shall be performed per power supply shock test procedure: :

Non-operating square wave shock

Acceleration	40	G
Duration	508	cm/Sec
Pulse	Square wave	
Number of Shock	All 6 sides tested	

Non-operating half-sine shock

Acceleration	142	G
Duration	178	cm/Sec
Pulse	Half sine wave	
Number of Shock	All 6 sides tested	

Operating half-sine shock

Acceleration	82	G
Duration	102	cm/Sec
Pulse	Half-Sine wave	
Number of Shock	All 6 sides except AC connection	

SECTION 5 POWER AND CONTROL SIGNAL DESCRIPTIONS

5.1 AC Input Connector

This connector supplies the AC Mains to the CSU3200AT series power supply.

- Pin 1 – L
- Pin 2 – N
- Pin 3 – Earth Ground

5.2 Output Connector – Power Blades

These pins provide the main output for the CSU3200AT series power supply. The Main Output (V_O) and the Main Output Return pins are the positive and negative rails, respectively, of the V_O main output of the CSU3200AT series power supply.

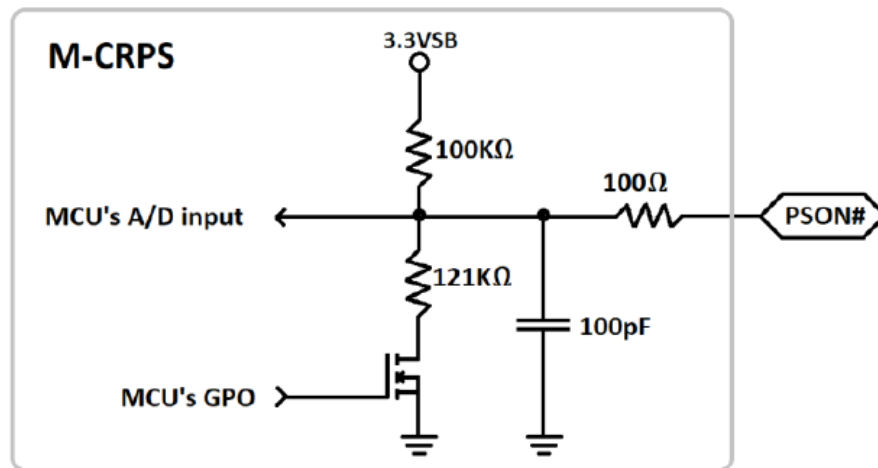
- A1-A9 (P1-P3) – Main Output Return
- A10-A18 (P4-P6) – Main Output (V_O)
- B1-B9 (P1-P3) – Main Output Return
- B10-B18 (P10-P12) – Main Output (V_O)

5.3 Output Connector – Control Signals

The CSU3200AT series power supply contains a 14 pins control signal header providing an analogue control interface, standby power and I²C interface signal connections.

PSON# - (Pin A21,S3)

This signal input pin controls the normal turn on and off of the main output of the CSU3200AT series power supply. It can be configured via firmware to work as a two-state (default) or multi-state PSON# signal based on the configuration provided by the configuration file. To accomplish the two/multi-state modes the power supply shall incorporate the circuit below.



Note 1 - Applying a logic 1 to the MOSFET will configure the PSON# input signal as multi-state.

Note 2 - Applying a logic 0 to the MOSFET will configure the PSON# input signal as two-state.

SECTION 5 POWER AND CONTROL SIGNAL DESCRIPTIONS

The specifications for these two different configurations are described in the following subsections.

Two-State Signal

When the PSON# signal is configured as two-state, it shall be active low to turn ON the +12V main power output. When this signal is not pulled low by the system, or left open, the +12V main output shall be turned OFF while the 12V_{SB} output shall remain ON. This signal is pulled to a standby voltage by a pullup resistor internal to the power supply. The table below lists the required characteristics of the PSON# signal when configured as two-state input.

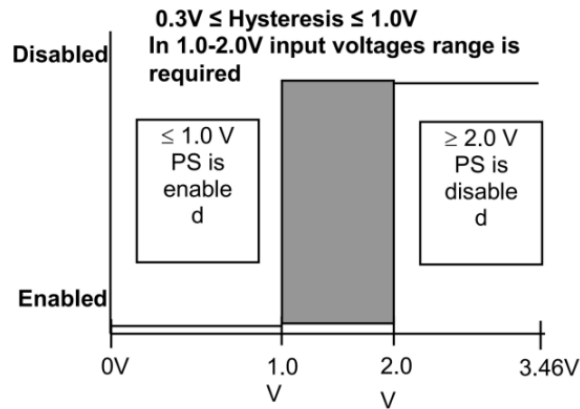


Table 10. Two-state PSON# signal characteristics

Signal Type	Accepts an open collector/drain input from the system. Pull-up to 3.3V _{SB} located in power supply.	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0 V	1 V
Logic level high (power supply OFF)	2 V	3.46 V
Source current, V _{pson} = low	-	4 mA
Power off delay: T _{pson_off_delay}	-	5 ms
Power up delay: T _{pson_on_delay}	5 ms	400 ms
PWOK delay: T _{pson_pwok}	-	5 ms

SECTION 5 POWER AND CONTROL SIGNAL DESCRIPTIONS

Multi-State Signal

When configured as multi-state input, the PSON# signal shall be able to detect logic 0, logic 1 and high impedance (pin floating). The thresholds to detect these three states are depicted in the following figure.

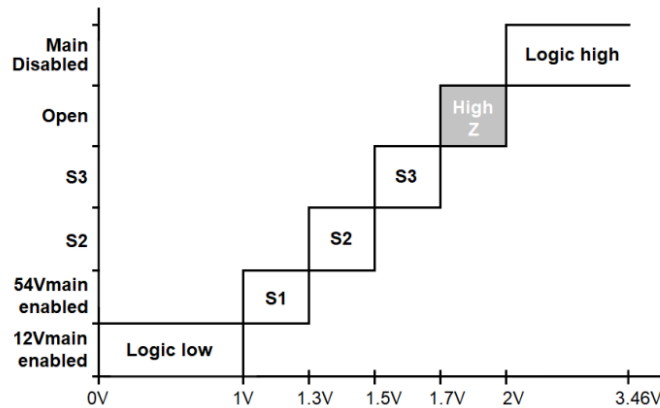


Table 11. Multi-state PSON# voltage ranges definition

State	Power supply must detect PSON# voltage within this range			System must set PSON# voltage within this range			12V M-CRPS Main output
	MIN(V)	NOM(V)	MAX(V)	MIN(V)	NOM(V)	MAX(V)	
Logic low	0	-	1	0	-	0.95	Main output ON, 12V _{SB} ON
S1	1	1.15	1.3	1.03	1.15	1.27	Main output OFF, 12V _{SB} ON
S2	1.3	1.4	1.5	1.33	1.4	1.47	Main output OFF, 12V _{SB} ON
S3	1.5	1.6	1.7	1.53	1.6	1.67	Main output OFF, 12V _{SB} OFF
Open	1.7	1.85	2	1.73	1.85	1.87	12V _{SB} ON ¹
Logic high	2	-	3.46	2.05	-	1.95	Main output OFF, 12V _{SB} ON

Note 1 – Please see [table 12](#) for the main output

SECTION 5 POWER AND CONTROL SIGNAL DESCRIPTIONS

PSON# stage designed to follow the logic as shown in the table below for assertion and deassertion states when used in Multi-state PSON# mode.

Table 12. PSON# transition states when using multi-state mode				
No.	VINOK	System State Of PSON#	PSON# Transition State	PSU Main Output State
1	High	Initialization (HI-Z, HIGH)	Hi-Z, High	Remain OFF
2	High	Low	Low	Stays ON
3			High	Turns OFF
4			HI-Z	Stays ON
5	High	High	Low	Turn ON
6			High	Remain OFF
7			HI-Z	Remain OFF
8	High	HI-Z	Low	Turn ON if OFF Remain ON
9			High	Turn Off if On Remain OFF
10			HI-Z	Preserve Last State
11	Low	Low	Low	Remain ON until PWOK drops
12			High	Turn off
13			HI-Z	Remain ON until PWOK drops
14	Low	High	Low	Turn ON until PWOK drops
15			High	Remain OFF
16			HI-Z	Remain OFF
17	Low	HI-Z	Low	Turn ON until PWOK drops
18			High	Turn Off if On Remain OFF
19			HI-Z	Preserve Last State

SECTION 5 POWER AND CONTROL SIGNAL DESCRIPTIONS

SMBALERT# - (Pin A22, S4)

SMBALERT indicates that the power supply is experiencing a problem that the user should investigate. This signal shall be asserted due to critical events or Warning events as configured in the configuration file. The signal shall activate in the case of critical component temperature reaching a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits. This SMBAlert# signal is to be asserted in parallel with LED color code selected in the configuration file.

Table 13. SMBAlert# signal characteristics		
Signal Type	Open collector / drain output from power supply. Pull-up to 3.3VSB located in the system.	
Alert# = High	OK	
Alert# = Low	Power alert to system	
	MIN	MAX
Logic level low voltage, Isink=4mA	0 V	0.4 V
Logic level high voltage, Isink=50uA		3.46 V
Sink current, alert# = low		4m A
Sink current, alert# = high		50 uA

PS_KILL - (Pins A23, S5)

The PS_KILL signal rapidly shuts down the main output or prevents the power supply from turning on before the PS_KILL signal contacts the system when the power supply is unplugged or plugged in without disconnecting the AC/DC power cord, thus preventing arcing at the connector. To achieve this, the PS_KILL pin is shorter than other signal pins at the card edge. The 12V_{SB} output should remain on as long as the input voltage remains within the specified range.

Table 14. PSKILL signal parameters	
Parameter	Specification
Delay between PSKILL signal being disconnected and PSU main output's ramping down	<100 us
Maximum voltage droop compensation	±200 mV

PWOK - (Pin A25,S7)

PWOK is a power OK output signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. See the table below for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall be inhibited as long as any power supply output is in current limit.

SECTION 5 POWER AND CONTROL SIGNAL DESCRIPTIONS

Table 15. PWOK signal characteristics

Signal Type	Open collector / drain output from power supply. Pull-up to 3.3V _{SB} located in the system.	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	MAX
Logic level low voltage, I _{sink} =400uA	0 V	0.4 V
Logic level high voltage, I _{source} =200uA	2.4 V	3.46 V
Sink current, PWOK = low	-	400 uA
Source current, PWOK = high	-	2 mA
PWOK delay: T _{pwok_on}	380 ms	420 ms
PWOK rise and fall time	-	100 us
Power down delay: T _{pwok_off}	1 ms	-
Any PSU fault to PWOK deassertion delay	-	100 us

12V_{SB} - (Pin B21,S10)

This pin provides the standby output for the CSU3200AT series power supply. The Standby Output (V_{SB}) and the GND pin are the positive and negative rails, respectively, of the V_{SB} of the CSU3200AT series power supply.

CR_BUS - (Pin B22,S11)

There is an additional signal defined supporting cold redundancy. This is connected to a bus shared between the power supplies and CR_BUS. This is a tri-state output signal of the power supply used to communicate a fault or V_{out} under-voltage level has occurred in one of the power supplies. This is used to power on all the power supplies in the system via the CR_BUS. When the signal is pulled high, it allows all power supplies in cold standby mode to go into cold standby state when the load share voltage is below the V_{CR_ON} level. When the signal is left open on all power supplies, it forces all cold standby power supplies into the ON. The cold redundancy section showing the logic state of the CR_BUS signal depending upon the programmed configuration of the power supply in D0h, the operating state of the power supply, and the power supply fault status.

ISHARE - (Pin B23, S12)

12V load share is a single wire bus signal used to help equalize the output current from two or more power supplies connected to a common load. The current share signal is a DC signal that represents the load current that a power supply is providing. This voltage increases proportionately with the output load. The expected voltage levels are stated as below table.

The ISHARE bus signal shall have a voltage setting of 8V at full load to accommodate a dynamic range of up to 16V for a 2x rated current measurement.

IMON - (Pin B24, S13)

The power supply shall incorporate an output current monitoring pin which will act as a current mirror of the main 12V output, I_{mon} signals from other power supplies in the system can be tied together to provide a mechanism for the system to measure the total output current of all the power supplies combined. The signal shall include an output diode to prevent the current from other power supplies' I_{mon} signal from entering a power supply that is not energized. The characteristics of the signal are described in the table.

SECTION 5 POWER AND CONTROL SIGNAL DESCRIPTIONS

Table 16. IMON signal parameters	
Signal Type	Current Source
Sensitivity (configurable via configuration file) ¹	0 to 2mA (representing 0 to 200% of rated current) or 10uA/A4 with a range of 0 to 200% of rated current.
Minimum bandwidth	40 kHz
Compliance voltage	3.3 V
Time constant	2.9 us to 4 us
Signal delay ²	<2 us
Input leakage ³	<500 nA

Note 1 - The IMON signal shall be able to provide information beyond PL4 levels.

Note 2 - Signal delay shall be tested using a load step from 0% to 100% and a di/dt of 10A/us without external capacitance connected to the power supply's main output.

Note 3 - Input leakage is defined when the power supply is not energized, when in standby state or when in cold redundant mode and it shall be guaranteed at 85°C and 12V.

VINOK - (Pin B25,S14)

VINOK signal indicates that the input voltage is within the range where the power supply can operate normally. Details of the operation are described in [Section 2.4 System Timing Requirements](#).

Table 17. VINOK signal characteristics		
Signal Type (Active High)	Open collector/drain output from power supply. 1K Ω Pull-up to 3.3VSB located in the power supply.	
VINOK = High	Input voltage is within the operational range	
VINOK = Low	Input voltage not within the operational range	
	MIN	MAX
Logic level low voltage, Isink=10mA	0 V	0.4 V
Logic level high voltage, Isource=4mA ¹	3 V	3.46 V
Sink current, VINOK = low		10 mA
Source current, VINOK = high		4 mA
VINOK rise and fall time		100 us

Note 1 - Using 100K Ω load resistor in the system side.

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

6.1 I²C Bus Signals

The CSU3200AT series power supply contains enhanced monitor and control functions implemented via the I²C bus. The CSU3200AT series I²C functionality (PMBus™ and FRU data) can be accessed via the output connector control signals. The communication bus is powered either by the internal 3.3V supply or from an external power source connected to the standby output (i.e. accessing an unpowered power supply as long as the standby output of another power supply connected in parallel is on).

If units are connected in parallel or in redundant mode, the standby outputs must be connected together in the system. Otherwise, the I²C bus will not work properly when a unit is inserted into the system without the DC source connected.

Note: PMBus™ functionality can be accessed only when the PSU is powered-up. Guaranteed communication I²C speed is 100KHz.

A0, A1 (PMBus Address Signals) - (Pins B19, S8)(Pins B20,S9))

The power supply shall be able to set its PMBus address and FRU address by checking the voltage levels in the A0 and A1 input pins, up to 4 PMBus addresses can be set combining logic states and analog voltage levels in these signals.

SDA, SCL (I²C Data and Clock Signals) - (Pins A19, S1)(Pins A20,S2)

I²C serial data and clock bus - these pins must be pulled-up by a 2.2K ohm resistor to 3.3V at the system side.

I²C Bus Communication Interval

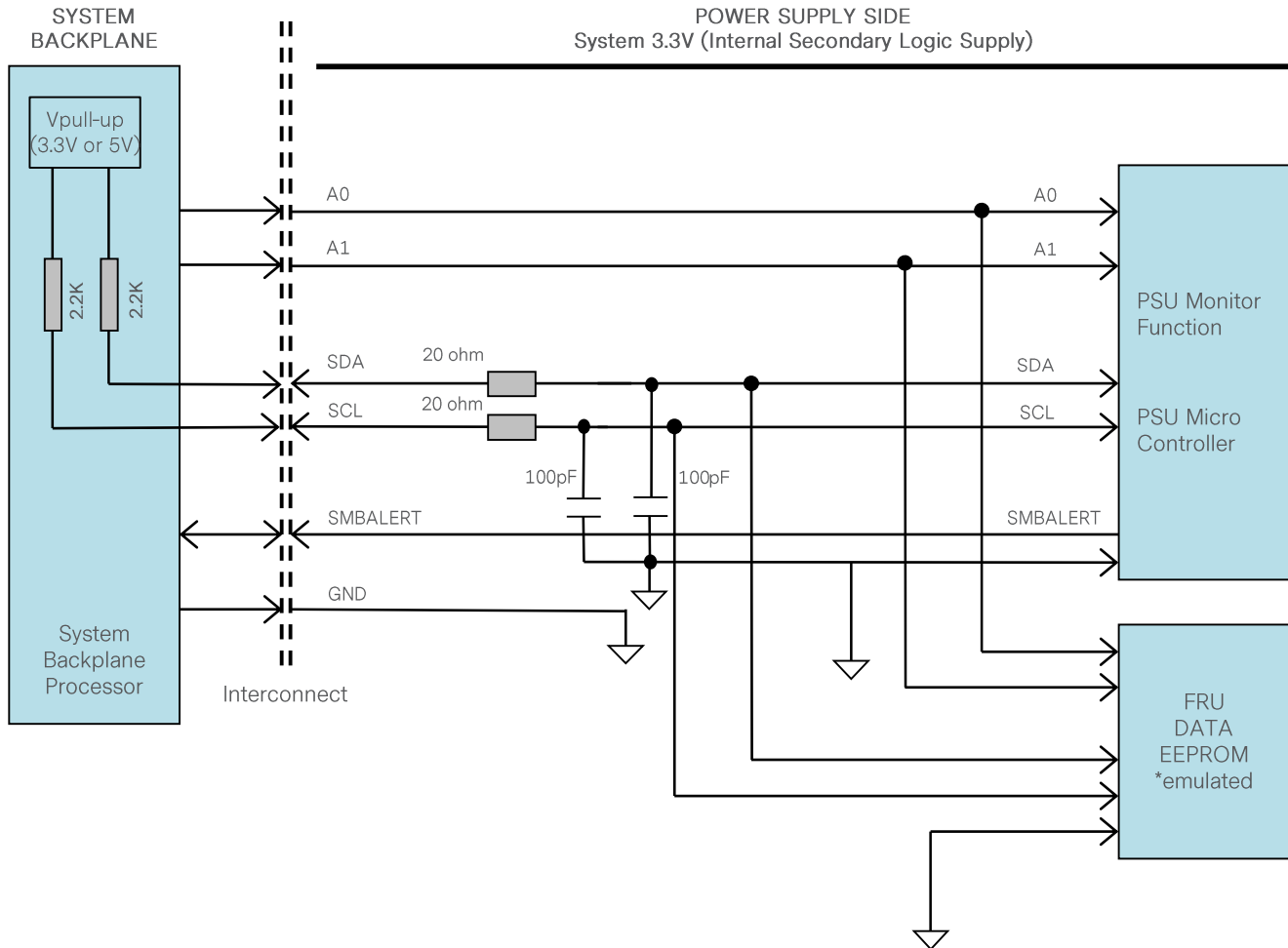
The interval between two consecutive I²C communications to the power supply must be at least 15ms to ensure proper monitoring functionality.

I²C Bus Signal Integrity

The noise on the I²C bus (SDA, SCL lines) due to the power supply will be less than 300mV peak-to-peak. This noise measurement should be made with an oscilloscope bandwidth limited to 100MHz. Measurements must be made at the power supply output connector with 2.2K ohm resistors pulled up to 3.3V source and a decoupling 47pF ceramic capacitors to standby output return.

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

I²C Bus Internal Implementation, Pull-ups and Bus Capacitances



I²C Bus - Recommended external pull-ups

Electrical and interface specifications of I²C signals (referenced to standby output return pin, unless otherwise indicated):

Parameter	Condition	Symbol	Min	Type	Max	Unit
SDA, SCL Internal Pull-up Resistor		R _{int}	-	-	100	Kohm
SDA, SCL Internal Bus Capacitance		C _{int}	-	-	100	pF
Recommended External Pull-up Resistor	1 to 4 PSU	R _{ext}	1	2.2	3	Kohm
Recommended External Pull-up Voltage		V _{pull-up}	3.3	-	5	V

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

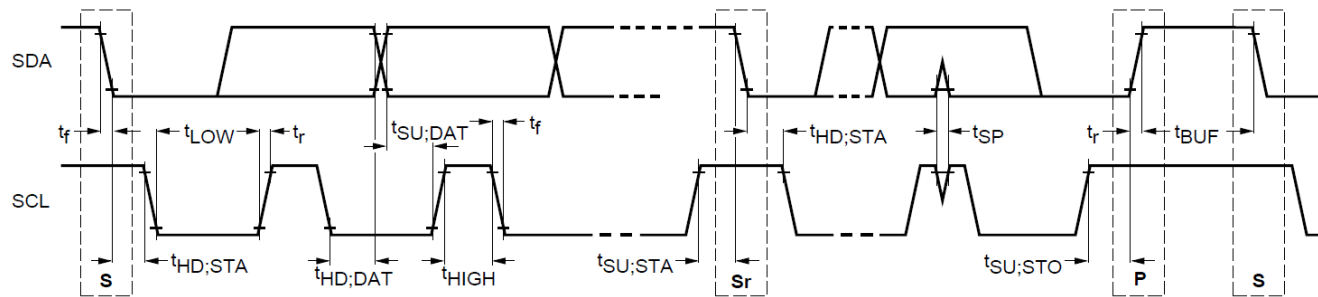
6.2 Logic Levels

CSU3200AT series power supply I²C communication bus will respond to logic levels as per below:

Logic High: 3.3V nominal (Spec is 2.1V to 5.5V)**

Logic Low: 500mV nominal (Spec is 800mV max)**

Timings



Parameter	Symbol	Standard-Mode Specs		Actual Measured		Unit
		Min	Max			
SCL clock frequency	f_{SCL}	10	400	58.80		KHz
Hold time (repeated) START condition	$t_{HD;STA}$	0.6	-	16.00		us
LOW period of SCL clock	t_{LOW}	1.3	-	9.6		us
HIGH period of SCL clock	t_{HIGH}	0.6	-	9.60		us
Setup time for repeated START condition	$t_{SU;STA}$	0.6	-	6.00		us
Data hold time	$t_{HD;DAT}$	300	-	5600		ns
Data setup time	$t_{SU;DAT}$	100	-	3400		ns
Rise time	t_r	20	-	SCL = 1600	SDA = 1200	ns
Fall time	t_f	20	-	SCL = 1400	SDA = 600	ns
Setup time for STOP condition	$t_{SU;STO}$	0.6	-	6.00		us
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	30.4		us

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

6.3 Device Addressing

The CSU3200AT series power supply will respond to supported commands on the PMbus that are addressed according to A1 and A0 pins of output connector.

Address pins are held HIGH by default via pulled up to internal 3.3V supply. To set the address as “0”, the corresponding address line needs be pulled down to logic ground level. Below tables show the address of the power supply with A0 and A1 pins set to either “0” or “1”.

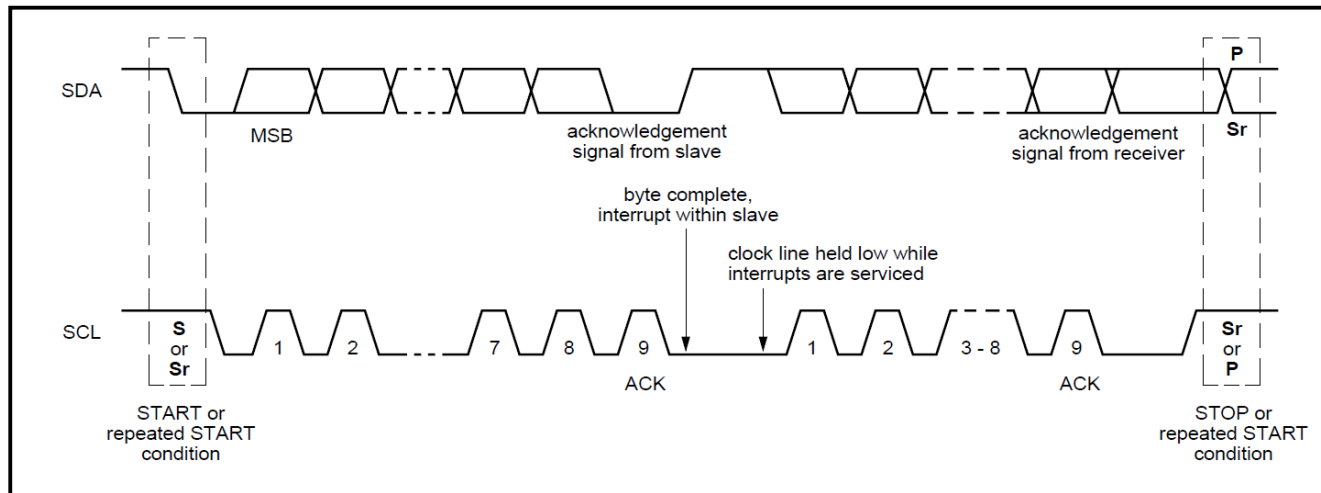
PSU Slot	Slot ID Bits		PMBus™ Address	EEPROM (FRU) Read Address
	A1	A0		
1	0	0	0xB0	0xA0
2	0	1	0xB2	0xA2
3	1	0	0xB4	0xA4
4	1	1	0xB6	0xA6

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

6.4 I²C Clock Synchronization

The CSU3200AT series power supply applies clock stretching. An addressed slave power supply holds the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The system master that is communicating with the power supply will attempt to raise the clock to transfer the next bit but must verify that the clock line was actually raised. If the power supply is clock stretching, the clock line will still be low (because the connections are open-drain).

The maximum time-out condition for clock stretching for CSU3200AT series is 30 milliseconds.



SECTION 6 COMMUNICATION BUS DESCRIPTIONS

6.5 Cold Redundancy

The CSU3200AT series power supply supports capabilities for cold redundancy. This capability helps improve the efficiency and iTHD of the power subsystem when more than one power supply is used in a system. Cold Redundancy uses the PMBus manufacturer specific command area to define PMBus commands for the system to communicate with the power supplies for enabling, configuration, and monitoring.

When configured as cold redundant, the power supply shall have a maximum input power of 4W when configured as cold redundant mode, input power shall be measured at the lowest nominal input voltage.

Overview

It covers both power supply and system requirements supporting redundant configurations of 1+1, 2+2, and 3+1.

When the power subsystem is in cold redundant mode; only the needed power supply to support the best power delivery efficiency are ON. Any additional power supplies, including the redundant power supply, are in cold standby state.

Each power supply has an additional signal that is dedicated to supporting cold redundancy; CR_BUS. This signal is a common bus between all power supplies in the system. CR_BUS is asserted (pulled low) when there is a fault in any power supply or the power supply's output voltage falls below the V_{fault} threshold. Asserting the CR_BUS signal causes all power supplies in the cold standby state to power ON.

Enabling power supplies to maintain best efficiency is achieved by looking at the Load Share bus voltage and comparing it to a programmed voltage level via a PMBus command.

Whenever there is no cold redundant active power supply on the cold redundancy bus driving a HIGH level on the bus all power supplies are ON no matter their defined cold redundant role (active or cold standby). This guarantees that incorrect programming of the cold redundancy states of the power supply will never cause the power subsystem to shutdown or become overloaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in cold redundant active state or standard redundant state to allow the cold standby state power supplies to go into cold standby state.

The following table shows the state of the power supplies programmed for cold standby mode based on the condition of the CR_BUS signal and the load share bus voltage.

Logic Matrix for Cold Standby Power Supplies:

CR_BUS	Load Share	Cold Standby Power Supply State
High	< VCR_ON	Cold Standby
Low	< VCR_ON	Active
High	> VCR_ON	Active
Low	> VCR_ON	Active

Note: VCR_ON is the voltage threshold set inside the power supplies configured for cold standby which tells them to power down into cold standby state when the load share voltage is less than VCR_ON.

When CR_BUS is asserted (pulled low), all power supplies in the system should go active and immediately provide power to the system.

SMBus Commands for Cold Redundancy

Configuring Cold Redundancy with Cold_Redundancy_Config (D0h)

The PMBus™ manufacturer specific command MFR_SPECIFIC_00 is used to configure the operating state of the power supply related to cold redundancy. This command for Cold_Redundancy_Config is D0h. The table below shows the configuration of the power supply based on the value in the Cold_Redundancy_Config register. PEC is used with the Read-Write Byte SMBus protocol.

The power supplies setup to be the cold standby power supplies shall change to standard redundancy mode (D0h = 00h) whenever the CR_BUS is pulled low.

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

Cold Redundancy Configuration Table

Cold_Redundancy_Config (D0h)		
Value	State	Description
00h	Standard Redundancy (Default Power on State)	Turns the power supply into standard redundant load sharing mode. The power supply's CR_BUS# signal shall be OPEN but still pull the bus low if a fault occurs to activate any power supplies still in Cold Standby state.
01h	Cold Redundant Active	Defines this power supply to be the one that is always ON in a cold redundancy configuration.
02h	Cold Standby 1	Defines the power supply that is the first to turn on in a cold redundant configuration as the load increases.
03h	Cold Standby 2	Defines the power supply that is the second to turn on in a cold redundant configuration as the load increases.
04h	Cold Standby 3	Defines the power supply that is the third to turn on in a cold redundant configuration as the load increases.
05h	Always Cold Standby	Defines this power supply to be always in cold redundant configuration no matter what the load condition.
06h	Cold Standby 4	Defines the power supply that is fourth to turn on in a cold redundant configuration as the load increases.
07h	Cold Standby 5	Defines the power supply that is fifth to turn on in a cold redundant configuration as the load increases.
08h	Cold Standby 6	Defines the power supply that is sixth to turn on in a cold redundant configuration as the load increases.
09h	Cold Standby 7	Defines the power supply that is seventh to turn on in a cold redundant configuration as the load increases.
0Ah	Cold Standby 8	Defines the power supply that is eighth to turn on in a cold redundant configuration as the load increases.
0Bh	Cold Standby 9	Defines the power supply that is ninth to turn on in a cold redundant configuration as the load increases.
0Ch	Cold Standby 10	Defines the power supply that is tenth to turn on in a cold redundant configuration as the load increases.
0Dh	Cold Standby 11	Defines the power supply that is eleventh to turn on in a cold redundant configuration as the load increases.
0Eh	Cold Standby 12	Defines the power supply that is twelfth to turn on in a cold redundant configuration as the load increases.
0Fh	Cold Standby 13	Defines the power supply that is thirteenth to turn on in a cold redundant configuration as the load increases.
10h	Cold Standby 14	Defines the power supply that is fourteenth to turn on in a cold redundant configuration as the load increases.
11h	Cold Standby 15	Defines the power supply that is fifteenth to turn on in a cold redundant configuration as the load increases.
12h – FFh	Reserved	

Note - When the CR_BUS transitions from a high to a low state; each power supply programmed to be in cold standby state shall be put into standard redundancy mode (Cold_Redundancy_Config = 00h). For the power supplies to enter cold redundancy mode the system must re-program the power supplies using the Cold_Redundancy_Config command.

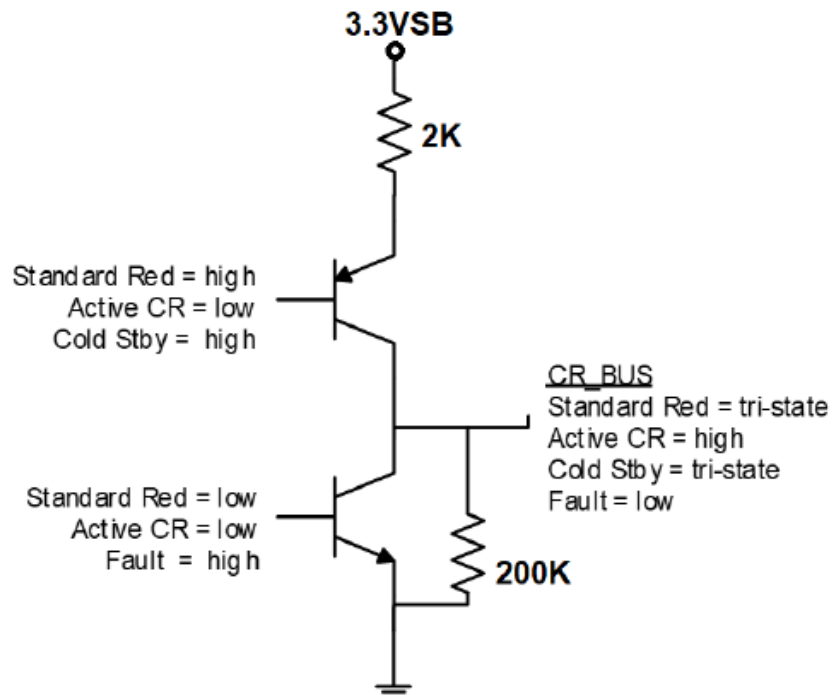
SECTION 6 COMMUNICATION BUS DESCRIPTIONS

Cold Redundant Signal (CR_BUS)

This is a tri-state output signal of the power supply used to communicate a fault or over current has occurred in one of the power supplies. This is used to power on all the power supplies in the system via the CR_BUS. When the signal is pulled high it allows all power supplies in cold standby mode to go into cold standby state when the load is light enough. When the signal is left open on all power supplies it forces them all cold standby power supplies ON.

Cold Redundancy State Table

Cold Redundant Config	Operating State	Power Supply Fault Status	CR_Bus#
Active	On	OK	High
Cold Standby 1,2,3	On	OK	Tri-state
Cold Standby 1,2,3	Cold Standby	OK	Tri-state
Always standby	Cold Standby	OK	Tri-state
Active	Off	Fault	Low
Cold Standby 1,2,3	On	Fault	Low
Cold Standby 1,2,3	Cold Standby	Fault	Low
Always standby	Cold Standby	Fault	Low



SECTION 6 COMMUNICATION BUS DESCRIPTIONS

CR_BUS Signal Characteristic

Signal Type	Value	
	Min	Max
Logic level low (power supply ON)	0V	Vil_cr_bus
Logic level high (power supply OFF)	Vih_cr_bus	-
Source current, Cold_Red = high	Ioh_cr_bus	-
Sink current, Cold_Red = low	-	Iol_cr_bus
Cold_Red fault delay	-	10us
Cold_Red turn on delay	-	100us

BMC Requirements

The BMC uses the COLD_REDUNDANCY_CONFIG command to define/configure the power supply's roll in cold redundancy and to turn on/off cold redundancy.

The BMC shall schedule a rolling change for which PSU is the Active, Cold Standby1, Cold Standby 2, and Cold Standby 3 power supply. The allows for equal loading across power supply over their life.

Events that trigger a re-configuration of the power supplies using the COLD_REDUNDANCY_CONFIG command.

- AC power ON
- PSON power ON
- Power Supply Failure
- Power supply inserted into system

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

6.6 Black Box

The power supply can store PMBus and other data into non-volatile memory upon a critical failure that caused the power supply to shut down. The data can be accessed via the PMBus interface by applying power to the 12V_{SB} pins. No AC power needs to be applied to the power supply.

Data is saved to the black box for the following fault events:

- Over current protection
- Over power protection
- Over temperature
- Over voltage protection on output
- Under voltage protection on output
- Over voltage protection on input
- Under voltage protection on input
- Fan failure
- PFC over voltage protection

Black Box Process:

- 1) System writes system tracking data to the power supply RAM at power ON.
- 2) System writes the real time clock data to the PSU RAM once every ~5 minutes.
- 3) Power supply tracks the number of PSON and AC power cycles in FLASH.
- 4) Power supply tracks ON time in FLASH.
- 5) Power supply loads warning and fault event counter data from FLASH into RAM.
- 6) Upon a warning event, the PSU will increment the associated counter in RAM.
- 7) Upon a fault event, the PSU will increment the associated counter in RAM.
- 8) Upon a fault event that causes the PSU to shut down, all event data in the PSU's RAM is saved to event data location N in the power supply's FLASH. This data includes the real time clock, the number of AC & PSON power cycles, PSU ON time, warning event counters and fault event counters.

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

Commands:

Name: MFR_BLACKBOX

Format: Read Block with PEC (238 bytes)

Code: DCh

	Item	Number of Bytes	Description
System tracking data	System top assembly number	10	The system will write its Intel part number for the system top assembly to the power supply when it is powered ON. This is 9 ASCII characters.
	System serial number	10	The system will write the system serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Motherboard assembly number	10	The system will write the motherboard Intel part number for the assembly to the power supply when it is powered ON. This is 9 ASCII characters.
	Motherboard serial number	10	The system will write the motherboard's serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Present total PSU ON time	3	Total on time of the power supply with PSON asserted in minutes. LSB = 1 minute.
	Present number of AC power cycles	2	Total number of times the power supply powered OFF then back ON due to loss of AC power. This is only counted when the power supply's PSON signal is asserted. This counter will stay at FFFFh once the max is reached.
	Present number of PSON power cycles	2	Total number of times the power supply is powered OFF then back ON due to the PSON signal de-asserting. This is only counted when AC power is present to the power supply. This counter will stay at FFFFh once the max is reached.
Power supply event data (N)		38	Most recent occurrence of saved black box data.
Time stamp			The power supply will track these time and power cycle counters in RAM. When the a black box event occurs the data is saved into the black box.
	Power supply total power on time	3	Total on time of the power supply in minutes. LSB = 1 minute.
	Real time clock data from system (Reserved for future use)	4	This time stamp does not need to generated by the power supply. The system rights a real time clock value periodically to the power supply using the MFR_REAL_TIME command. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1 second resolution past the year 2100. This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C.
	Number of AC power cycles	2	Number of times the power supply powered OFF then back ON due to loss of AC power at the time of the event. This is only counted when the power supply's PSON signal is asserted.
	Number of PSON power cycles	2	Number of times the power supply is powered OFF then back ON due to the PSON signal deasserting at the time of the event. This is only counted when AC power is present to the power supply.

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

	Item	Number of Bytes	Description
PMBus			The power supply will save these SMBus values into the black box when a black box event occurs. Fast events may be missed due to the filtering effects of the PMBus sensors.
	STATUS_WORD	2	
	STATUS_IOUT	1	
	STATUS_INPUT	1	
	STATUS_TEMPERATURE	1	
	STATUS_FAN_1_2	1	
	READ_VIN	2	
	READ_IIN	2	
	READ_IOUT	2	
	READ_TEMPERATURE_1	2	
	READ_TEMPERATURE_2	2	
	READ_FAN_SPEED_1	2	
	READ_PIN	2	
	READ_VOUT	2	
Event counters			The power supply will track the total number for each of the following events. These value will be saved to the black box when a black box event occurs. Once a value has reached 15, it will stay at 15 and not reset.
	AC shutdown due to under voltage on input	Lower ½	The power supply will save a count of these critical events to non-volatile memory each time they occur. The counters will increment each time the associated STATUS bit is asserted.
	Thermal shutdown	Upper ½	
	Over current or over power shutdown on output	Lower ½	
	General failure shutdown	Upper ½	
	Fan failure shutdown	Lower ½	
	Shutdown due to over voltage on output	Upper ½	
	Input voltage warning; no shutdown	Lower ½	The power supply will save into RAM a count of these warning events. Events are count only at the initial assertion of the event/bit. If the event persists without clearing the bit the counter will not be incremented. When the power supply shuts down it will save these warning event counters to non-volatile memory. The counters will increment each time the associated STATUS bit is asserted.
	Thermal warning; no shutdown	Upper ½	
	Output current power warning; no shutdown	Lower ½	
	Fan slow warning; no shutdown	Upper ½	
	Power supply event data (N-1)	38	
	Power supply event data (N-2)	38	
	Power supply event data (N-3)	38	
	Power supply event data (N-4)	38	

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

Name: MFR_REAL_TIME_BLACK_BOX
 Format: Write/Read Block with PEC (4 bytes)
 Code: DDh

The system will use this command to periodically write the real time clock data to the power supply.

Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1 second resolution past the year 2100.

This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C.

Name: MFR_SYSTEM_BLACK_BOX
 Format: Write/Read Block with PEC (40 bytes). Low byte first.
 Code: DEh

The system uses this command to write the following data to the PSU.

Item	Bytes	
System top assembly number	1–10	Low bytes
System serial number	11–20	
Motherboard assembly number	21–30	
Motherboard serial number	31–40	High bytes

Name: MFR_BLACKBOX_CONFIG
 Format: Read/Write Byte with PEC
 Code: DFh

Bit	Value	Description
0	0 = disable black box function 1 = enable black box function	Writing a '1' enables the power supply with black box function. Writing a '0' disables the power supply black box function. The state of MFR_BLACKBOX_CONFIG will be saved in non-volatile memory so that it is not lost during power cycling. Intel will receive the power supply with the black box function enabled; bit 0 = '1'.
1-7		reserved

Name: MFR_CLEAR_BLACKBOX
 Format: Send Byte with PEC
 Code: E0h

The MFR_CLEAR_BLACKBOX command is used to clear all black box records simultaneously. This command is write only. There is no data byte for this command.

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

6.7 FRU (EEPROM) Data

The FRU (Field Replaceable Unit) data format is compliant with the Intel IPMI v1.0 specification.

The CSU3200AT series uses 1 page of EEPROM for FRU purpose. A page of EEPROM contains up to 256 byte-sized data locations.

Where:	OFFSET	-The OFFSET denotes the address in decimal format of a particular data byte within CSU3200AT series EEPROM.
	VALUE	-The VALUE details data written to a particular memory location of the EEPROM.
	DEFINITION	-The contents DEFINITION refers to the definition of a particular data byte.

CSU3200AT series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
COMMON HEADER, 8 BYTES				
0	00	FORMAT VERSION NUMBER (Common header) 7:4 - Reserved, write as 0000b 3:0 - Format version number = 1h for this specification	1	01
1	01	INTERNAL USE AREA OFFSET (Not required, do not reserve)	0	00
2	02	CHASSIS INFO AREA OFFSET (Not required, do not reserve)	0	00
3	03	BOARD INFO AREA OFFSET (Not required, do not reserve)	0	00
4	04	PRODUCT INFO AREA OFFSET	4	04
5	05	MULTI RECORD AREA OFFSET	18	12
6	06	PAD (Not required, do not reserve)	0	00
7	07	ZERO CHECK SUM (256 - (Sum of bytes 0 to 6))	233	E9
8	08	(08h-1Fh is Reserved, default value is 0.)	0	00
9	09		0	00
10	0A		0	00
11	0B		0	00
12	0C		0	00
13	0D		0	00
14	0E		0	00
15	0F		0	00
16	10		0	00
17	11		0	00
18	12		0	00
19	13		0	00
20	14		0	00
21	15		0	00
22	16		0	00
23	17		0	00
24	18		0	00
25	19		0	00
26	1A		0	00
27	1B		0	00
28	1C		0	00
29	1D		0	00
30	1E		0	00
31	1F		0	00
PRODUCT INFORMATION AREA, 128 BYTES				
32	20	FORMAT VERSION NUMBER (Product Info Area) 7:4 - Reserved, write as 0000b 3:0 - Format Version Number = 1h for this specification	1	01

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

CSU3200AT series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
33	21	PRODUCT INFO AREA LENGTH	14	0E
34	22	Language (English)	25	19
35	23	MANUFACTURER NAME TYPE / LENGTH (CCH) 3:2 - (11)b, ASCII code 1:0 - (00)b, 12 bytes allocation	204	CC
36	24	MANUFACTURER'S NAME 12 bytes sequence "A" = 41h "E" = 45h "I" = 49h	65	41
37	25		69	45
38	26		73	49
39	27		32	20
40	28		32	20
41	29		32	20
42	2A		32	20
43	2B		32	20
44	2C		32	20
45	2D		32	20
46	2E		32	20
47	2F		32	20
48	30	PRODUCT NAME Type/Length 7:6 - (00)b, ASCII code 5:0 - (100100)b, 36 bytes allocation	228	E4
49	31	Product Name, 36 bytes sequence "MCRPS: Common Redundant Power Supply " In Decimal = 077d, 067d, 082d, 080d, 083d, 058d, 032d, 067d, 111d, 109d, 109d, 111d, 110d, 32d, 82d, 101d, 100d, 117d, 110d, 100d, 97d, 110d, 116d, 32d, 80d, 111d, 119d, 101d, 114d, 32d, 83d, 117d, 112d, 112d, 108d, 121d In Hex = 4DH, 43H, 52H, 50H, 53H, 3AH, 20H, 43H, 6FH, 6DH, 6DH, 6FH, 6EH, 20H, 52H, 65H, 64H, 75H, 6EH, 64H, 61H, 6EH, 74H, 20H, 50H, 6FH, 77H, 65H, 72H, 20H, 53H, 75H, 70H, 70H, 6CH, 79H	77	4D
50	32		67	43
51	33		82	52
52	34		80	50
53	35		83	53
54	36		58	3A
55	37		32	20
56	38		67	43
57	39		111	6F
58	3A		109	6D
59	3B		109	6D
60	3C		111	6F
61	3D		110	6E
62	3E		32	20
63	3F		82	52
64	40		101	65
65	41		100	64
66	42		117	75
67	43		110	6E
68	44		100	64
69	45		97	61
70	46		110	6E
71	47		116	74
72	48		32	20
73	49		80	50
74	4A		111	6F
75	4B		119	77
76	4C		101	65
77	4D		114	72
78	4E		32	20
79	4F		83	53
80	50		117	75
81	51		112	70
82	52		112	70
83	53		108	6C
84	54		121	79

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

CSU3200AT series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
85	55	PRODUCT PART/MODEL NUMBER Type/Length (10H) 7:6 - (11)b, ASCII code 5:0 - (010000)b, 16-byte allocation	208	D0
86	56	Part / Model Number "CSU3200AT-3-3M0 " In Decimal = 067d, 083d, 085d, 051d, 050d, 048d, 048d, 065d, 084d, 045d, 051d, 045d, 051d, 077d, 048d, 032d In Hex = 43H, 53H, 55H, 33H, 32H, 30H, 30H, 41H, 54H, 2DH, 33H, 2DH, 33H, 4dH, 30H, 32H	67	43
87	57		83	53
88	58		85	55
89	59		51	33
90	5A		50	32
91	5B		48	30
92	5C		48	30
93	5D		65	41
94	5E		84	54
95	5F		45	2D
96	60		51	33
97	61		45	2D
98	62		51	33
99	63		77	4D
100	64		48	30
101	65		32	20
102	66	PRODUCT VERSION NUMBER Type/Length (10h) 7:6 - (11)b, ASCII code 5:0 - (010000)b, 16-byte allocation	208	D0
103	67	Version , 16 bytes sequence	48	30
104	68		32	20
105	69		32	20
106	6A		32	20
107	6B		32	20
108	6C		32	20
109	6D		32	20
110	6E		32	20
111	6F		32	20
112	70		32	20
113	71		32	20
114	72		32	20
115	73		32	20
116	74		32	20
117	75		32	20
118	76		32	20
119	77	PRODUCT SERIAL NUMBER Type/Length 7:6 - (11)b, ASCII code 5:0 - (001110)b, 14-byte allocation	208	D0
120	78	Serial number , 16 bytes sequence "XXXXXXXXXXXXXXXX"	XX	XX
121	79		XX	XX
122	7A		XX	XX
123	7B		XX	XX
124	7C		XX	XX
125	7D		XX	XX
126	7E		XX	XX
127	7F		XX	XX
128	80		XX	XX
129	81		XX	XX
130	82		XX	XX
131	83		XX	XX
132	84		XX	XX
133	85		XX	XX

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

CSU3200AT series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE			
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)		
134	86	Serial number, 16 bytes sequence	XX	XX		
135	87		XX	XX		
136 137 138 139 140 141 142	88	PAD (reserved) Default value is 0. Default value is 0.	0	00		
	89		0	00		
	8A		193	C1		
	8B		0	00		
	8C		0	00		
	8D		0	00		
	8E		0	00		
143	8F	ZERO CHECK SUM (256-(sum of bytes 32 to 135)) Per Unit Zero Check Sum: should follow check sum calculation as per IPMI v1.3 specs	NA	NA		
MULTI RECORD AREA, 96 BYTES						
144 145 146 147 148	90	Power Supply Record Header				
	91	Record type = 00 for power supply info	0	00		
	92	End of list / Record format version number for 12V output record	2	02		
	93	Record length of 12V output record	24	18		
	94	Record checksum	NA	NA		
		Header checksum	NA	NA		
POWER SUPPLY RECORD						
149 150	95 96	Combined Wattage, byte 1 and byte 2: 3200W = 0C80H Byte 1 (LSB) = 80h = 128d Byte 2 (MSB) = 0Ch = 12d 2 bytes sequence In Decimal = 128d, 12d In Hex = 80h,0Ch	128 12	80 0C		
		151 152	97 98	Peak VA, 3400W = 0D48H 2 bytes sequence In Decimal = 13d, 72d In Hex = 0DH, 48H	72 13	48 0D
				153	99	Inrush Current, 35A In Decimal = 35d In Hex = 23H
154	9A	Inrush Interval, 255mS In Decimal = 255d In Hex = FFH	255	FF		
155 156	9B 9C	Low End Input Voltage Range 1(10mV), (90V/10mV) 9000=2328H 2 bytes sequence Byte 1 (LSB) = 28h Byte 2 (MSB) = 23h	40 35	28 23		
		157 158	9D 9E	High End Input Voltage Range 1(10mV), (240V/10mV) 26400=6720H 2 bytes sequence In Decimal = 32d, 103d In Hex = 20H, 67H	32 103	20 67
159 160	9F A0			Low End Input Voltage Range 2(10mV), (180V/10mV) 0000=0000H 2 bytes sequence In Decimal = 00d, 00d In Hex = 00H, 00H	0 0	00 00
		161 162	A1 A2	High End Input Voltage Range 2(10mV), (240V/10mV) 0000=0000H 2 bytes sequence In Decimal = 00d, 00d In Hex = 00H, 00H	0 0	00 00
163	A3			Low End Input Frequency Range	0	00
164	A4	High End Input Frequency Range	60	3C		

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

CSU3200AT series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
165	A5	AC Dropout Tolerance in ms, 12ms = 0CH	12	0C
166	A6	Binary Flags: For each of the following binary flags No = 0, Yes = 1. Bits 7-5: RESERVED, Write as 000b Bit4: Tachometer Pulses Per Rotation / Predictive Fail Polarity BIT = 0 Bit3: Hot Swap / Redundancy Support BIT = 1 Bit2: Auto switch Support BIT = 0 Bit1: Power Factor Correction Support BIT = 1 Bit0: Predictive Fail Support BIT = 1	11	0B
167	A7	Peak Wattage Capacity and Holdup Time, (Set for 3500Watts/15S) In Decimal = 172 In Hex = ACH (LSB First)	172	AC
168	A8	In Decimal = 253 In Hex = FDH	253	FD
169	A9	Combined Wattage, byte 1 and byte 2: 3200W = 0C80H Byte 1 (LSB) = 80h = 128d Byte 2 (MSB) = 0Ch = 12d	0	00
170	AA	2 bytes sequence In Decimal = 128d, 12d	128	80
171	AB	In Hex = 80h,0Ch	12	0C
172	AC	Predictive Fail Tachometer Lower Threshold, Not Applicable. Predictive failure is not supported.	0	00
12V OUTPUT RECORD HEADER				
173	AD	Record Type = 01 for power supply info	1	01
174	AE	End of List / Record Format Version Number for 12V Output Record	2	02
175	AF	Record Length of 12V Output Record	13	0D
176	B0	Record checksum	NA	NA
177	B1	Header checksum	NA	NA
12V OUTPUT RECORD				
178	B2	Output Information, 000 = 00H Bit 7: Standby information = 0b Bits 6-5: Reserved, write as 000b Bits 4: Current units, 0b = 10mA Bits 3-0: Output number 0 = 000b	0	00
179	B3	Nominal Voltage (10mV), (12.2V / 10mV) 1220 = 04C4H 2 bytes sequence In Decimal: 196d, 004d	196	C4
180	B4	In Hex: C4H, 04H	4	04
181	B5	Maximum Negative Voltage Deviation (12.11V / 10mV), 1211 = 04BBH 2 bytes sequence In Decimal: 187d, 004d	187	BB
182	B6	In Hex: BBH, 04H	4	04
183	B7	Maximum Positive Voltage Deviation (12.29V / 10mV), 1229 = 04CDH 2 bytes sequence In Decimal: 205d, 004d	205	CD
184	B8	In Hex: CDH, 04H	4	04
185	B9	Ripple and Noise pk-pk (mV), 120 = 78H 2 bytes sequence In Decimal: 120d, 000d	120	78
186	BA	In Hex: 78H, 00H	0	00

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

CSU3200AT series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
187	BB	Minimum Current Draw (mA) , 1000 = 03E8H 2 bytes sequence In Decimal: 232d, 003d In Hex: E8H, 03H	232	E8
188	BC		3	03
189	BD	Maximum Current Draw (mA) , 65535 = FFFFH 2 bytes sequence In Decimal: 255d, 255d In Hex: FFH, FFH	255	FF
190	BE		255	FF
12VSB OUTPUT RECORD HEADER				
191	BF	Record type = 01 for DC Output Record	1	01
192	C0	End of List / Record Format Version Number for 12V _{SB} Output Record	2	02
193	C1	Record Length of 12V DC Output Record	13	0D
194	C2	Record CHECKSUM of 12V _{SB} Output Record	NA	NA
195	C3	Header CHECKSUM of 12V _{SB} Output Record Header	NA	NA
12VSB OUTPUT RECORD				
196	C4	Output Information , 129 = 81H Bit 7: Standby Information = 1b Bits 6-4: Reserved, write as 000b Bits 3-0: Output number 1 = 0001b	129	81
197	C5	Nominal Voltage (10mV) , (12V / 10mV) 1200 = 04B0H 2 bytes sequence In Decimal: 176d, 004d In Hex: B0H, 04H	176	B0
198	C6		4	04
199	C7	Maximum Negative Voltage Deviation (10mV) , 1140 = 0474H 2 bytes sequence In Decimal: 116d, 004d In Hex: 74H, 04H	116	74
200	C8		4	04
201	C9	Maximum Positive Voltage Deviation (10mV) , 1260 = 04ECH 2 bytes sequence In Decimal: 236d, 004d In Hex: ECH, 04H	236	EC
202	CA		4	04
203	CB	Ripple and Noise pk-pk (mV) , 120 = 78H 2 bytes sequence In Decimal: 120d, 000d In Hex: 78H, 00H	120	78
204	CC		0	00
205	CD	Minimum Current Draw (10mA) , 0000 = 0000H 2 bytes sequence In Decimal: 000d, 000d In Hex: 00H, 00H	0	00
206	CE		0	00
207	CF	Maximum Current Draw (10mA) , 3500 = 0DACH 2 Bytes Sequence In Decimal: 172d, 13d In Hex: ACH, 0DH	172	AC
208	D0		13	0D
M-CRPS IDENTIFIER HEADER				
209	D1	Record type = C2	194	C2
210	D2	End of List / Record Format Version Number	139	8B
211	D3	Record Length	27	1B
212	D4	Record CHECKSUM	NA	NA
213	D5	Header CHECKSUM	NA	NA
M-CRPS IDENTIFIER				
214	D6	Manufacturer ID	0	00
215	D7		0	00
216	D8		0	00
217	D9	Record Version	1	01

SECTION 6 COMMUNICATION BUS DESCRIPTIONS

CSU3200AT series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
218	DA	M-CRPS Revision [15:8] – Major number = 01h [7:0] – Minor number = 00h	1	01
219	DB		0	00
220	DC	M-CRPS Version [7:4] – Major number [3:0] – Minor number	16	10
221	DD	M-CRPS Type [7:4] – Input [3:0] – Output	0	00
222	DE	M-CRPS Outline 00h – 73.5 x 185.0 mm 01h – 73.5 x 265.0 mm 02h – 60.0 x 185.0 mm	0	00
223	DF	M-CRPS Cooling Type [7:4] – Cooling [3:0] – Temperature range	0	00
224	E0	M-CRPS Efficiency Titanium	4	04
225	E1	OEM	0	00
226	E2		0	00
227	E3		0	00
228	E4		0	00
229	E5		0	00
230	E6		0	00
231	E7		0	00
232	E8		0	00
233	E9		0	00
234	EA		0	00
235	EB		0	00
236	EC		0	00
237	ED		0	00
238	EE		0	00
239	EF		0	00
240	F0		0	00
241	F1	Reseved	0	00
242	F2		0	00
243	F3		0	00
244	F4		0	00
245	F5		0	00
246	F6		0	00
247	F7		0	00
248	F8		0	00
249	F9		0	00
250	F1A		0	00
251	FB		0	00
252	FC		0	00
253	FD		0	00
254	FE		0	00
255	FF		0	00

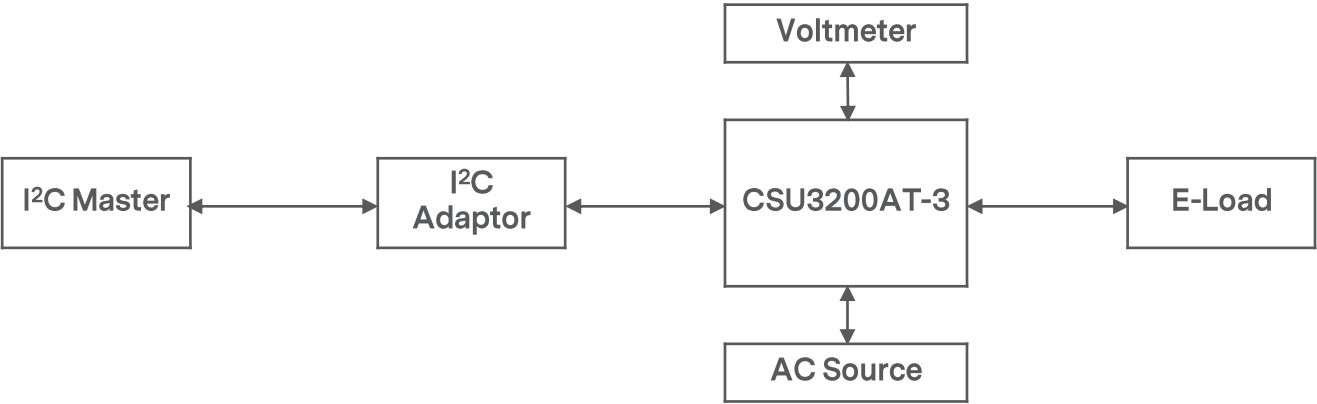
SECTION 7 PMBus™ SPECIFICATIONS

The CSU3200AT series is compliant with the industry standard PMBus™ protocol for monitoring and control of the power supply via the I²C interface port.

7.1 CSU3200AT Series PMBus™ General Instructions

Equipment Setup

The following is typical I²C communication setup:



I²C Accuracy

Output Load	Vout	Eout	Pout	Temp	Fan speed
<6.56 A	±2%	-	-	±2%	±250 RPM
6.56 to 13.12 A	±2%	-	±10%	±2%	±250 RPM
13.12 to 26.23 A	±2%	±2%	±7%	±2%	±250 RPM
26.23 to 52.46 A	±2%	±2%	±5%	±2%	±250 RPM
52.46 to 131.15 A	±2%	±2%	±2%	±2%	±250 RPM
131.15 to 262.3 A	±2%	±2%	±2%	±2%	±250 RPM

SECTION 7 PMBus™ SPECIFICATIONS

The CSU3200AT Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
00h	PAGE	00	R/W	1	Hex	Valid input: 00h, 01h, FFh
01h	OPERATION	00	R/W	1	Bitmapped	80 - Turn On 40 - Turn Off
02h	ON_OFF_CONFIG	15	R/W	1	Bitmapped	15 - Only support PSON to turn on/off PSU 18 - PSU could turn on/off by PSON and operation command 01h
03h	CLEAR_FAULTS	NA	W		N/A	
05h	PAGE_PLUS_WRITE	Variable	BW	Variable	N/A	
06h	PAGE_PLUS_READ	Variable	BWR	Variable	N/A	
10h	WRITE_PROTECT	00	R/W	1	Bitmapped	
11h	Reserved					
12h	Reserved					
15h	Reserved					
16h	Reserved					
19h	CAPABILITY	B0	R	1	Bitmapped	Provides a way for the hosts system to determine some key capabilities of a SMBus™ device.
	b7 - Packet Error Checking					0 - PEC not supported 1 - PEC supported
	b6:5 - Maximum Bus Speed					00 - Maximum supported bus speed, 100KHz 01 - Maximum supported bus speed, 400KHz 10 - Maximum supported bus speed, 1MHz 11 - Reserved
	b4 - SMBALERT#					0 - PMBus Alert Pin not supported 1 - PMBus Alert Pin supported
	b3 - Numeric Format					0 - Linear11, Ulinear16, Slinear16, or Direct 1 - IEEE half precision floating point format
	b2 - AVSBus					0 - AVSBus not supported 1 - AVSBus supported
	b1:0					Reserved
1Ah	QUERY	Variable	BWR	2	Bitmapped	Supported in ISP mode
1Bh	SMBALERT_MASK	Variable	WW/BWR	2	Bitmapped	Default masks per Intel spec: Page 00: STATUS_VOUT = FFh STATUS_IOUT = FFh STATUS_INPUT = FFh STATUS_TEMP = FFh STATUS_CML = FFh Page 01: STATUS_VOUT = FFh STATUS_IOUT = DFh STATUS_INPUT = EFh STATUS_TEMP = BFh STATUS_CML = FFh Non-paged: STATUS_FANS_1_2 = FFh

SECTION 7 PMBus™ SPECIFICATIONS

The CSU3200AT Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
20h	Reserve					
21h	Reserve					
22h	Reserve					
24h	Reserve					
25h	Reserve					
26h	Reserve					
27h	Reserve					
28h	Reserve					
29h	Reserve					
2Ah	Reserve					
30h	COEFFICIENTS	05 01 00 00 00 00	BWR	6	Hex	Use to retrieve the m, b and R coefficients, needed for DIRECT data format.
	b5					R byte
	b4:3					b low byte, b high byte
	b2:1					m low byte, m high byte
33h	FREQUENCY_SWITCH	00	R	1	Hex	
35h	VIN_ON	F2C8	R	2	Linear	
36h	VIN_OFF	F2AC	R	2	Linear	
38h	Reserved		R			
39h	Reserved		R			
3Ah	FAN_CONFIG_1_2	80	R/W	1	Bitmapped	
	b7	1				0 - No fan is installed in position 1. 1 - Fan is installed in position 1.
	b6	0				0 - Fan is commanded in DC. 1 - Fan is commanded is RPM.
	b5:4	00				00 - 1 pulse per revolution 01 - 2 pulse per revolution 10 - 3 pulse per revolution 11 - 4 pulse per revolution
3Bh	FAN_COMMAND_1	0	R/W	2	Linear	Adjusts the operation of the Fans in RPM/DC. The device may override the command, if it requires higher value to maintain proper device temperature.
40h	VOUT_OV_FAULT_LIMIT	1BE6	R	2	Linear	
41h	VOUT_OV_FAULT_RESPONSE	80	R	1	Bitmapped	
42h	VOUT_OV_WARN_LIMIT	1B00	R	2	Linear	
43h	VOUT_UV_WARN_LIMIT	1380	R	2	Linear	
44h	VOUT_UV_FAULT_LIMIT	1380	R	2	Linear	
45h	VOUT_UV_FAULT_RESPONSE	80	R	1	Bitmapped	
46h	IOUT_OC_FAULT_LIMIT	FADE	R	2	Linear	
47h	IOUT_OC_FAULT_RESPONSE	80	R	1	Bitmapped	
4Ah	IOUT_OC_WARNING_LIMIT	FAAA	R/W	2	Linear	
4Fh	OT_FAULT_LIMIT	F21C	R	2	Linear	
50h	OT_FAULT_RESPONSE	80	R	1	Bitmapped	
51h	OT_WARN_LIMIT (Hot Spot)	EBD8	R/W	2	Linear	Secondary ambient temperature warning threshold, in degree C. Operating limit

SECTION 7 PMBus™ SPECIFICATIONS

The CSU3200AT Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
55h	VIN_OV_FAULT_LIMIT	FA44	R	2	Linear	
56h	VIN_OV_FAULT_RESPONSE	80	R	1	Bitmapped	
57h	VIN_OV_WARN_LIMIT	FA3A	R	2	Linear	
58h	VIN_UV_WARN_LIMIT	F2BC	R	2	Linear	
59h	VIN_UV_FAULT_LIMIT	F2AC	R	2	Linear	
5Ah	VIN_UV_FAULT_RESPONSE	80	R	1	Bitmapped	
5Dh	IIN_OC_WARN_LIMIT	08 40 DA 40 DA 40 DA 40 CA	R	9	N/A	
6Bh	PIN_OP_WARN_LIMIT	1372	R	2	Linear	
78h	STATUS_BYTE	00	R	1	Bitmapped	Returns the summary of critical faults.
	b7 - BUSY					Not supported.
	b6 - OFF					Unit is off.
	b5 - VOUT_OV_Fault					Output over-voltage fault has occurred.
	b4 - IOUT_OC_Fault					Output over-current fault has occurred.
	b3 - VIN_UV_Fault					An input under-voltage fault has occurred.
	b2 - TEMPERATURE					A temperature fault or warning has occurred.
	b1 - CML					A communication, memory or logic fault has occurred.
	b0 - NONE OF THE ABOVE					Not supported
79h	STATUS_WORD	0000	R	2	Bitmapped	Summary of fault and warning status.
	b15 - VOUT					An output voltage fault or warning has occurred.
	b14 - IOUT/POUT					An output current or power fault or warning has occurred.
	b13 - INPUT					An input voltage, current or power fault or warning as occurred.
	b12 - MFR_SPECIFIC					
	b11 - POWER_GOOD#					The POWER_GOOD (PWOK) signal is de-asserted.
	b10 - FANS					A fan or airflow fault or warning has occurred.
	b6 - OFF					Unit is off.
	b5 - VOUT_OV_Fault					Output over-voltage fault has occurred.
	b4 - IOUT_OC_FAULT					Output over-current fault has occurred.
	b3 - VIN_UV_FAULT					An input under-voltage fault has occurred.
	b2 - TEMPERATURE					A temperature fault or warning has occurred.
	b1 - CML					A communication, memory or logic fault has occurred.

SECTION 7 PMBus™ SPECIFICATIONS

The CSU3200AT Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
7Ah	STATUS_VOUT	00	R/W	1	Bitmapped	
	b7 - VOUT Over-Voltage Fault					VOUT over-voltage fault
	b6 - VOUT_OV_WARNING					
	b5 - VOUT_UV_WARNING					
	b4 - VOUT Under-Voltage Fault					VOUT under-voltage fault
7Bh	STATUS_IOUT	00	R/W	1	Bitmapped	
	b7 - IOUT Overcurrent Fault					IOUT overcurrent fault
	b5 - IOUT Overcurrent Warning					IOUT overcurrent warning
	b1 - POUT_OP_FAULT					POUT overpower fault
	b0 - POUT_OP_WARNING					POUT overpower warning
7Ch	STATUS_INPUT	00	R/W	1	Bitmapped	Input related faults and warnings
	b7 - VIN_OV_FAULT					Not supported
	b6 - VIN_OV_WARNING					VIN over-voltage warning
	b5 - VIN_UV_WARNING					VIN under-voltage warning
	b4 - VIN_UV_FAULT					VIN under-voltage fault
	b3 - Unit Off For Low Input Voltage					Unit is off for insufficient input voltage.
	b1 - IIN_OC_WARNING					IIN overcurrent warning
	b0 - PIN_OP_WARNING					PIN overpower warning
7Dh	STATUS_TEMPERATURE	00	R/W	1	Bitmapped	Temperature related faults and warnings
	b7 - Over Temperature Fault					Over temperature fault
	b6 - Over Temperature Warning					Over temperature warning
7Eh	STATUS_CML	00	R/W	1	Bitmapped	
	b7 - Invalid/Unsupported command					
	b6 - Invalid/Unsupported Data					
	b5 - Packet Error Check Failed					
	b4 - Memory Fault Detected					
	b3 - Processor Fault Detected					
	b2 - Reserved					
	b1 - A communication fault other than the ones listed in this table has occurred					
	b0 - Other Memory Or Logic Fault has occurred					
7Fh	STATUS_OTHER	00	R/W	1	Bitmapped	
80h	STATUS_MFR_SPECIFIC	00	R/W	1	Bitmapped	
	b4 - Power supply line status change					Asserted when the power supply detects a line status condition change
	b2 - High Line input, power derated					Asserted when the power supply has a lower voltage than the required for full power at high line.

SECTION 7 PMBus™ SPECIFICATIONS

The CSU3200AT Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
81h	STATUS_FANS_1_2	00	R/W	1	Bitmapped	
	b7 - Fan1 Fault					Fan1 Fault
	b6 - Fan2 fault					Fan2 Fault
	b5 - Fan1 Warning					Fan1 Warning
	b4 - Fan2 Warning					Fan2 Warning
86h	READ_EIN	Variable	BR	7	Direct	Returns the accumulated input power over time.
87h	READ_EOUT	Variable	BR	7	Direct	Returns the accumulated output power over time.
88h	READ_VIN	Variable	R	2	Linear	Returns input voltage in Volts ac.
89h	READ_IIN	Variable	R	2	Linear	Returns input current in Amperes.
8Ah	READ_VCAP	Variable	R	2	Linear	Returns input current in capacitance.
8Bh	READ_VOUT	Variable	R	2	Linear16	Returns the actual, measured voltage in Volts.
8Ch	READ_IOUT	Variable	R	2	Linear	Returns the output current in amperes.
8Dh	READ_TEMPERATURE_1	Variable	R	2	Linear	Returns the ambient temperature in degree celsius.
8Eh	READ_TEMPERATURE_2	Variable	R	2	Linear	Returns the hot pot temperature in degree celsius.
8Fh	READ_TEMPERATURE_3	Variable	R	2	Linear	Returns the exhaust temperature in degree celsius.
90h	READ_FAN_SPEED_1	Variable	R	2	Linear	Speed of fan 1
91h	READ_FAN_SPEED_2	NA	R	2	Linear	Speed of fan 2 (not support)
94h	READ_DUTTY_CYCLE	0x32	R			
96h	READ_POUT	Variable	R	2	Linear	Returns the output power, in Watts.
97h	READ_PIN	Variable	R	2	Linear	Returns the input power, in Watts.
98h	PMBus_REVISION	0x22	R	1	Bitmapped	Reads the PMBus revision number.
	b7:5					Part 1 Revision 0000 - Revision 1.0 0001 - Revision 1.1 0010 - Revision 1.2
	b4:0					Part 2 Revision 0000 - Revision 1.0 0001 - Revision 1.1 0010 - Revision 1.2
99h	MFR_ID	Variable	BR	13	ASCII	
9Ah	MFR_MODEL	Variable	BR	17	ASCII	Supported in ISP mode Model number matching label.
9Bh	MFR_REVISION	Variable	BR	17	ASCII	
9Ch	MFR_LOCATION	Variable	BR	17	ASCII	
9Dh	MFR_DATE	YY/MM/DD	BR	7	N/A	
9Eh	MFR_SERIAL	Variable	BR	15	ASCII	
9Fh	APP_PROFILE_SUPPORT	0x05	R	1	ASCII	
A0h	MFR_VIN_MIN	0x00B4	R	2	Linear	
A1h	MFR_VIN_MAX	0x0108	R	2	Linear	
A2h	MFR_IIN_MAX	0xDA40	R	2	Linear	

SECTION 7 PMBus™ SPECIFICATIONS

The CSU3200AT Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
A3h	MFR_PIN_MAX	0x1372	R	2	Linear	Maximum input Power
A4h	MFR_VOUT_MIN	0x1614	R	2	Linear	Minimum Output voltage
A5h	MFR_VOUT_MAX	0x19EC	R	2	Linear	Maximum output voltage
A6h	MFR_IOUT_MAX	0xFA0D	R	2	Linear	Maximum output current
A7h	MFR_POUT_MAX	0x1320	R	2	Linear	Maximum output power
A8h	MFR_TAMBIENT_MAX	0x0037	R	2	Linear	
A9h	MFR_TAMBIENT_MIN	0x07FB	R	2	Linear	
ADh	IC_DEVICE_ID	04 39 30 00 00	BR	5	N/A	
AEnh	IC_DEVICE_REV	04 14 00 00 00	BR	5	N/A	
B0h	Reserve		BWR			
B1h	Reserve		BWR			
B2h	Reserve		BWR			
B3h	MFR_EFFICIENCY_DATA	3200W: input type, 4W, 85%, 90%, 94%, 95%, 95.5%, 96%, 95%, 94%, 93%, 92%, 91%	BR	46	N/A	
B4h	Reserve		BWR			
B8h	Reserve		BWR			
C0h	MFR_MAX_TEMP_1	0xE3C0	R	2	Linear	
C1h	MFR_MAX_TEMP_2	0xEBD8	R	2	Linear	
C2h	MFR_MAX_TEMP_3	0xEBD8	R	2	Linear	
D0h	MFR_COLD_REDUNDANCY_CONFIG	0x00	R/W	1	Hex	
D1h	MFR_READ_CONFIG_FILE_SIZE	03 00 28 00	BR	4	N/A	
D2h	MFR_READ_CONFIG_BLOCK_SIZE	0x0010	R	2	Hex	
D3h	MFR_READ_CONFIG_FILE	Variable	BWR	17	N/A	
D4h	MFR_HW_COMPATIBILITY	02 00	R	2	Bitmapped	
D5h	MFR_FWUPLOAD_CAPABILITY	0x04	R	1	Bitmapped	
D6h	MFR_FWUPLOAD_MODE	00	R/W	1	Bitmapped	
D7h	MFR_FWUPLOAD	Variable	BW	Variable	N/A	
D8h	MFR_FWUPLOAD_STATUS	00	R	2	Bitmapped	
D9h	MFR_FW_REVISION	Variable	BR	8	Hex	
DAh	MFR_SPDM	Variable	BWR	Variable	N/A	
DBh	MFR_FRU_PROTECTION	01	R/W	1	Bitmapped	
DCh	MFR_BLACKBOX	Variable	BR	238	N/A	
DDh	MFR_REAL_TIME_BLACK_BOX	Variable	BWR	5	N/A	
DEh	MFR_SYSTEM_BLACK_BOX	Variable	BWR	41	N/A	
DFh	MFR_BLACKBOX_CONFIG	0x01	R/W	1	Bitmapped	
E0h	MFR_CLEAR_BLACKBOX	NA	W	1		
E1h	MFR_LINE_STATUS	Variable	R/W	1	Bitmapped	
E2h	MFR_SYSTEM_LED_CNTL	0x0007	R/W	2	Bitmapped	

SECTION 7 PMBus™ SPECIFICATIONS

The CSU3200AT Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
E3h	Reserve		Reserved			
E4h	Reserve		Reserved			
E5h	Reserve		Reserved			
E6h	Reserve		Reserved			
E9h	MFR_PEAK_CURRENT_RECORD	Variable	BWR	5	N/A	
EBh	MFR_COMPONENT_ID	04 B5 BB 01 00	BR	5	N/A	
ECh	MFR_TOT_POUT_MAX	0x1320	R	2	Linear	
EDh	MFR_VOUT_MARGINING	00 00	R/W	2	Bitmapped	
EEh	MFR_OCWPL1_SETTING	05 0C 54 05 E8 F3	BWR	6	N/A	
F0h	MFR_PWOK_WARNING_TIME	0xBACC	R/W	2	Linear	Power OK warning time
F1h	MFR_MAX_IOUT_CAPABILITY	0E 0D FA 5B FA 20 4E 2D FB 0A 00 62 FB 28 23	BR	15	N/A	
F2h	MFR_FPC_MAIN_MIN_OFF_TIME	0001	R/W	2	Linear	Main output's minimum OFF time
F3h	MFR_FPC_12VSB_MIN_OFF_TIME	0001	R/W	2	Linear	Standby output's minimum OFF time
FEh	MFR_SPECIFIC_COMMAND_EXT	N/A	N/A	N/A	N/A	Customer specific command set extension

SECTION 7 PMBus™ SPECIFICATIONS

Data Format: Linear11

Linear11 is linear data format used for the non output voltage related PMBus commands, for example output current, input voltage, input current, temperature, etc.

Linear data format follows the equation: $X = Y \times 2^N$

Where: X = real world data in decimal

Y = 11-bit transmitted value / mantissa

N = 5-bit exponent

Convert Linear Data Format to Real World Data

The following steps show how to convert from linear data format to its corresponding real world data.

1. Convert data from hex format to binary format.

Ex. The reading of 88h command (READ_VIN) is F398 hex, in Binary = 1111001110011000.

2. Separate the exponent N from the mantissa Y.

The format is aaaaaBBBBBBBBBBB

Where: a is binary format of exponent N = aaaaa = 11110

B is binary format of mantissa Y = BBBBBBBBBB = 01110011000

3. Convert exponent N from binary format to its corresponding decimal format.

N = 11110, convert to two's complement, it is -2 in decimal.

N = -2

4. Convert mantissa Y from binary format to its corresponding decimal format.

Y = 01110011000, convert to decimal, Y = 920.

5. Solve for the real world data X using below equation.

$$X = Y \times 2^N$$

$$= 920 \times 2^{-2}$$

$$= 230\text{VAC}$$

SECTION 7 PMBus™ SPECIFICATIONS

Data Format: Linear16

Linear16 is linear data format used for the output voltage related PMBus commands.

Linear data format follows the equation: Voltage = $V \times 2^N$

Where: Voltage = real world data in decimal

V = 16-bit transmitted value / mantissa

N = exponent depends on the VOUT_MODE command 20h

Convert Linear Data Format to Real World Data

The following steps show how to convert from linear data format to its corresponding real world data.

1. Find the VOUT_MODE command value of CSU3200AT, that is 17h.

Mode	Bits [7:5] (mode)	Bits [4:0] (Parameter)
Linear	000b	Five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.

2. Calculate N according to above table. 17h is 00010111 in binary.
Convert bits [4:0] 10111 to two's complement, it is -9 in decimal.
 $N = -9$
3. Ex. The reading of 8Bh READ_VOUT command is 1866 hex. Convert to decimal directly. It is 6246 decimal.
 $V = 6246$
4. Solve for the real world data X using below equation.

$$X = V \times 2^N$$

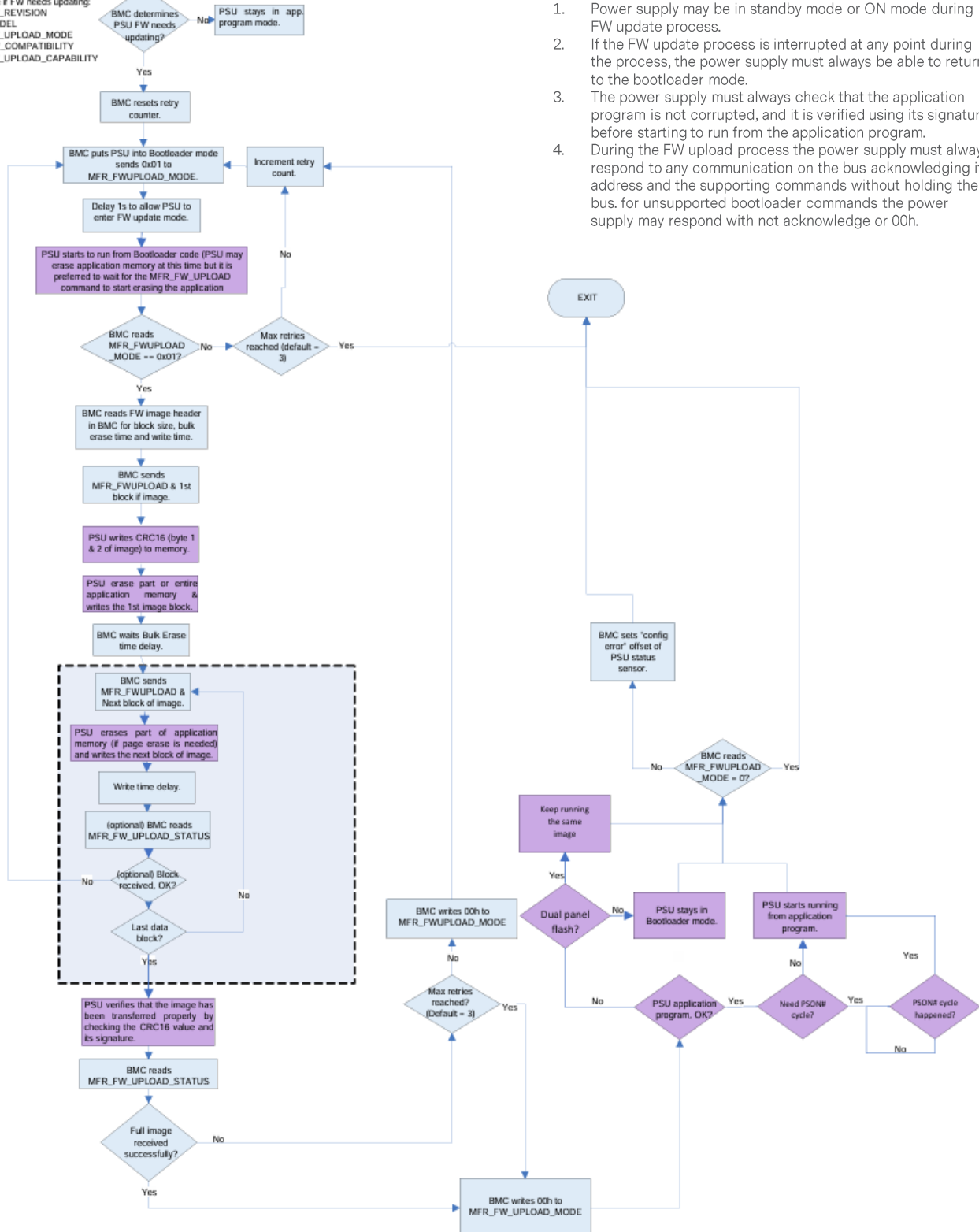
$$= 6246 \times 2^{-9}$$

$$= 12.2\text{VDC}$$

SECTION 7 PMBus™ SPECIFICATIONS

7.2 Firmware Update Process

BMC uses these commands to determine if FW needs updating:
MFR_FW_REVISION
MFR_MODEL
MFR_FW_UPLOAD_MODE
MFR_FW_COMPATIBILITY
MFR_FW_UPLOAD_CAPABILITY

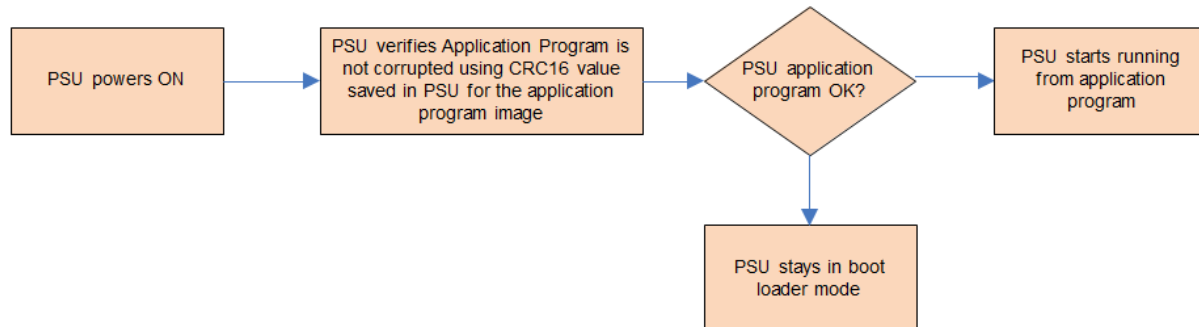


Notes:

1. Power supply may be in standby mode or ON mode during FW update process.
2. If the FW update process is interrupted at any point during the process, the power supply must always be able to return to the bootloader mode.
3. The power supply must always check that the application program is not corrupted, and it is verified using its signature before starting to run from the application program.
4. During the FW upload process the power supply must always respond to any communication on the bus acknowledging its address and the supporting commands without holding the bus, for unsupported bootloader commands the power supply may respond with not acknowledge or 00h.

SECTION 7 PMBus™ SPECIFICATIONS

7.3 PSU Flow During Powering ON



SECTION 8 FIRMWARE SECURITY

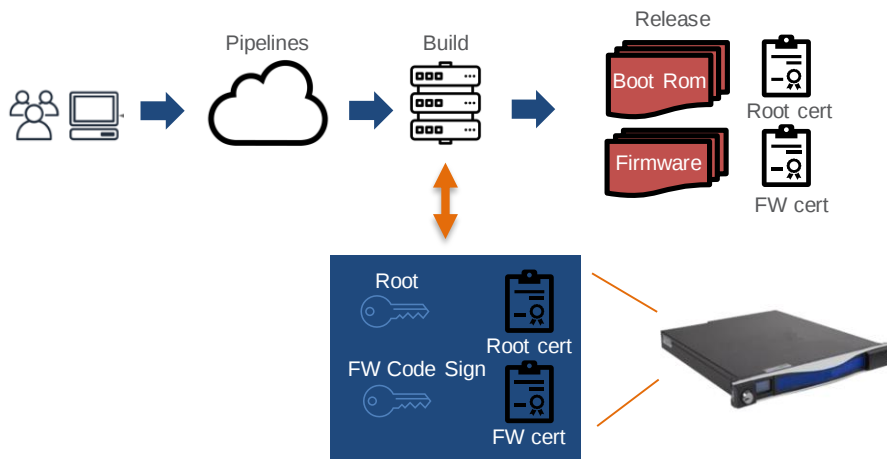
8.1 MCRPS Product Cyber Security Overview

Advanced Energy's MCRPS design requiring product level security

1. New security protocol implemented on top of the PMBus
2. Asymmetric cryptography utilized in provisioning
3. Hardware root of trust
4. Security verified by 3rd party testing

The power supply offers 3 system cyber security capabilities

1. Secure boot
2. Runtime measurements
3. Secure update



Benefits to Advanced Energy and the customer

1. Only Advanced Energy generated and signed firmware will be allowed to update and run on the device enforced via integrity protections
2. Customer can increase their system level security by doing a cryptographic check of the unit's runtime code

SECTION 8 FIRMWARE SECURITY

8.2 Algorithms, Certificates, and Key Storage

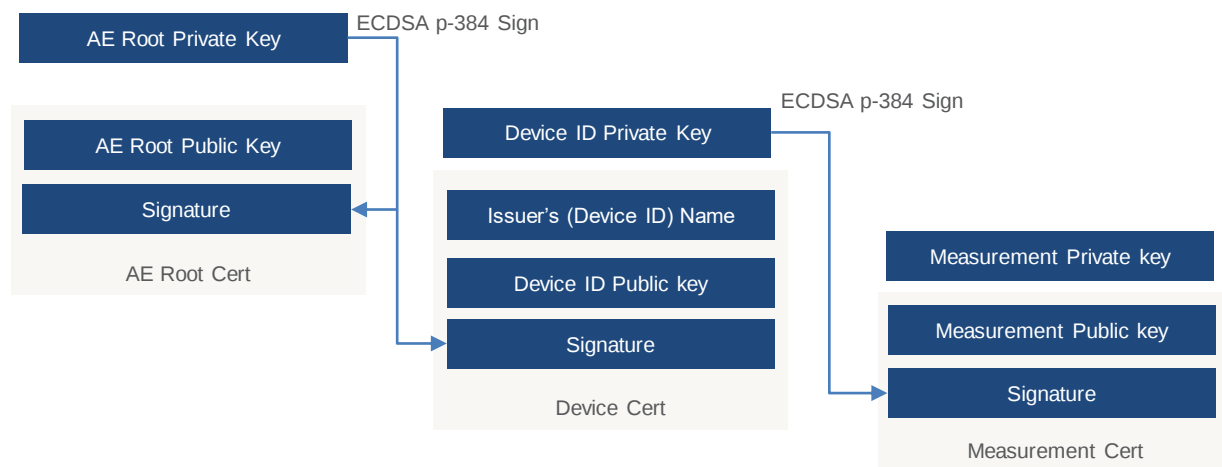
Meets the standard for Crypto algorithms

1. ECDSA P-384 - sign and verify operations
2. SHA2-384 - hashes mutable code digest and measurements

Hardware security module (HSM) storage of Advanced Energy's private key (FIPs-140 Compliant)

1. Allows for generation of certificates and secure update images
2. Enables a secure boot signed by the private key verified with the public key

Chained certificates implemented as hardware rooted security & key storage solution



Public Key Format

-----BEGIN CERTIFICATE-----

```

MIICGzCCAAcGAWIBAgIUxYutG3ZOatWMAX+t2b4/43tRvaggCgYIKoZlZj0EAwMw
PDEoMCYGA1UECgwQWR2YW5jZWQgRW5lcmd5IEluZHVzdHJpZXMsIEluYzEQMA4G
A1UEAwWUUm9vdCBDQTAeFw0yNDA5MTgyMjE2MTIaFw00OTA5MTkyMjE2MThaMDwx
KDAmbGhNVBAoMH0FkdMfuY2VkiEVuZXJneSBjbmR1c3RyaWVzLCBjbMxEdAOBgNV
BAMMB1Jvb3QgQ0EwdjAQBgcqhkiOPQIBBgUrgQQAIGNiAAQBB9vMDCnPlDtyn6FC
yPKVFFCrWI36/0jcaEiCaIX/gwQYmmukmur2BfQZA5MPkOyf/m2yQmA0Fb4ZhaC9
MtpoLm/ijR9AGrwyb9AlzE7uzDYpsrRsHDxEO3n3kPMgL6SjYzBhMA8GA1UdEwEB
/wQFMAMBAf8wHwYDVR0jBBgwFoAut7TobYUUIU0Lt5rep5pIEEvAJs8wHwYDVR0O
BBYEFLe06G2FJZVNC7ea3qeaSBBLwCbPMA4GA1UdDwEB/wQEAwIBhjAKBgqhkiO
PQQDAwNpADBmAJEAgIF6p1Rw8gb7GZfCxcfc3LnWMyriYzjEN/alELbMLfAylIO
aDglEcwQsEAGg3e/AjEAhFWPYKbHtW43LgJ8ts1kq4Egax5Tz1rBvf84R9iSo/y4
kin0E3E2flbcYdtViKop
  
```

-----END CERTIFICATE-----

SECTION 8 FIRMWARE SECURITY

8.3 Runtime Software Attestation

Runtime Attestation is:

Hash of the active code base used to assure to the system that the PSU is only running code authorized by Advanced Energy

Hardware SPDm protocol defines the process for obtaining measurements

1. SPDm is a message protocol implemented on top of the PMBus modeled between a secure requester (BMC) and secure responder (PSU)
2. BMC sends a challenge (random number) to be signed, wants hashes (measurements) of MCU app code, configuration file hash, and certificates returned
3. One way authentication, PSU is not looking to authenticate the BCM

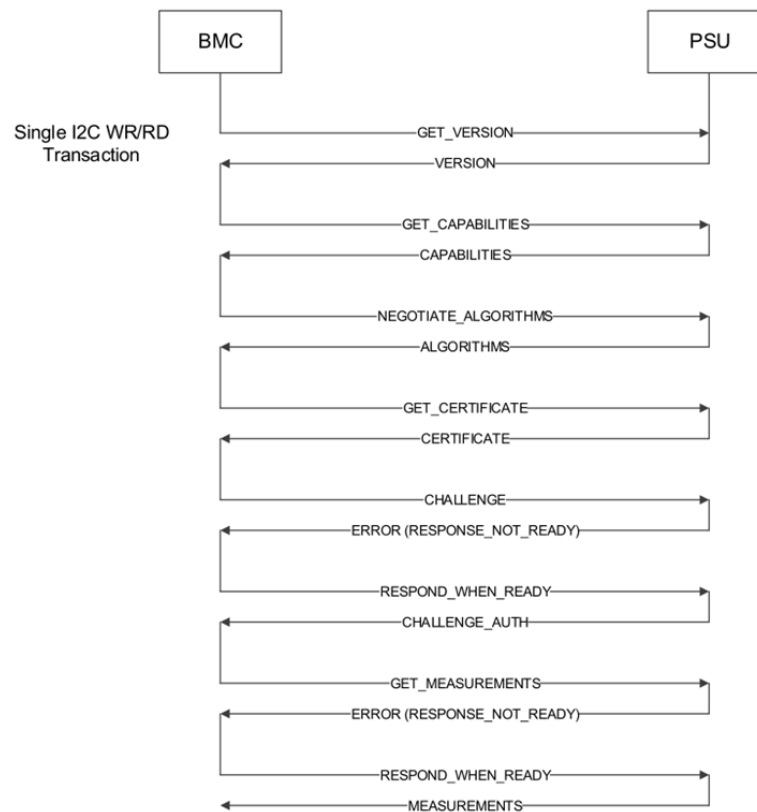


Figure 12-44 General SPDm Request/Response Flow

Challenge is used to see if the PSU has the private key associated with the measurement public key

1. Way to check for the presence of the key without needing to see the actual key
2. Measurement and device ID keys are chained in certificates and stored in the system

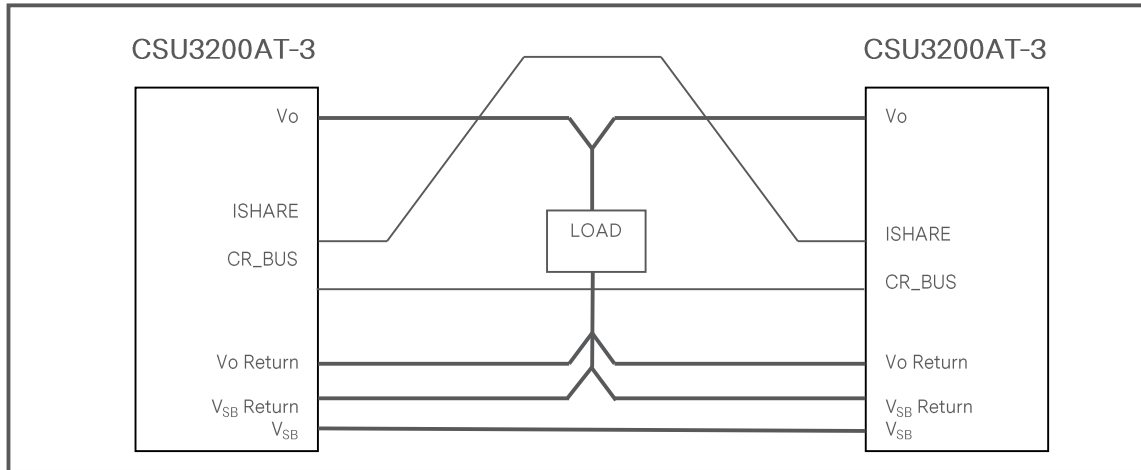
Required in the specification but up to the customer to use the measurement

Advanced Energy's public key certificate is available for the BMC to check if a PSU is from us

SECTION 9 APPLICATION NOTES

9.1 Current Sharing

The CSU3200AT main output V_O is equipped with current sharing capability. At 3+3 redundant power supply system, the +12V output with active current sharing and droop have maximum Current Share Error (CSE) of 4% from 5% to 100% of rated power. Redundant backup one of the power failures cannot affect other power supply operations and outputs. If ISHARE pin is short-circuited to the ground evenly, the power supply output should meet the specification.



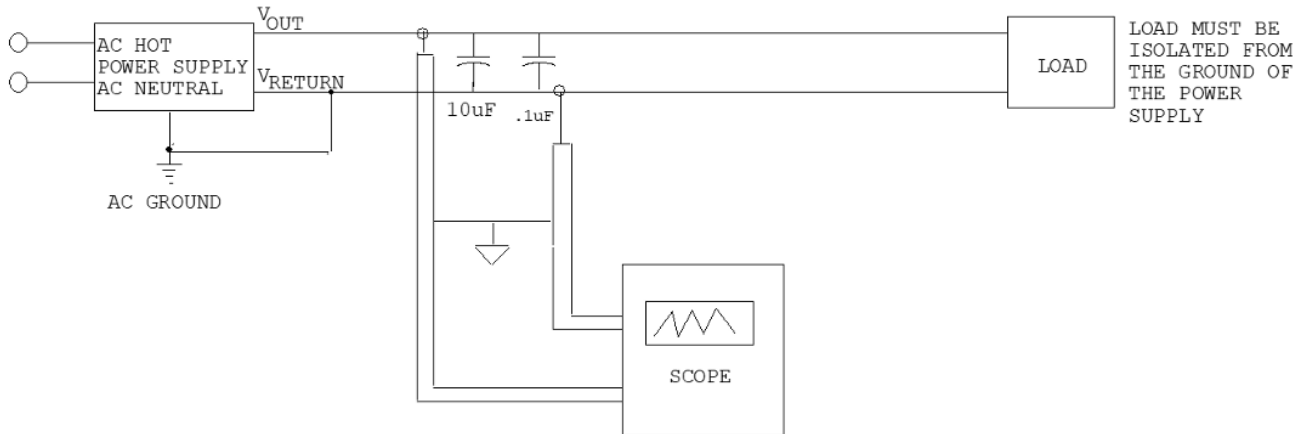
The power supplies must be able to share current with any combination of 1 to 6 PSUs in the system. Maximum output power for systems with “n” PSU of “W” power each, in parallel: $1*W + 0.95*(n-1)*W$.

PSU SKUs	Number of Supplies	Maximum System Power Rating
1+0	1	100% of One PSU Rating
1+1	2	100% of One PSU Rating
2+0	2	$100\% + (95\% \times 1) \times \text{PSU Rating}$
2+1	3	$100\% + (95\% \times 1) \times \text{PSU Rating}$
2+2	4	$100\% + (95\% \times 1) \times \text{PSU Rating}$
3+0	3	$100\% + (95\% \times 2) \times \text{PSU Rating}$
3+1	4	$100\% + (95\% \times 2) \times \text{PSU Rating}$
3+2	5	$100\% + (95\% \times 2) \times \text{PSU Rating}$
3+3	6	$100\% + (95\% \times 2) \times \text{PSU Rating}$

SECTION 9 APPLICATION NOTES

9.2 Output Ripple and Noise Measurement

The setup outlined in the diagram below has been used for output voltage ripple and noise measurements on the CSU3200AT-3-3M0. When measuring output ripple and noise, a scope jack in parallel with a 0.1uF ceramic chip capacitor, and a 10uF tantalum capacitor will be used. The oscilloscope can be set to 10Hz to 20MHz bandwidth for this measurement.



Note 1 – Use a Tektronix 7834 oscilloscope with 7A13 and differential probe P6055 or equivalent.

Note 2 - When performing this test, the probe clips and capacitors should be located close to the power supply connector.

Note 3 - Perform a load sweep from minimum load up to 100% in 10% load increments. Using a time/div of 10ms and 10us/div.

SECTION 10 RECORD OF REVISION AND CHANGES

Issue	Date	Description	Originators
1.0	07.23.2026	First issue	Zoey Yasheng

Note – The product is compliant to Open Compute Project M-CRPS 1p04.
Note – If you have any feedback for this document, feel free to contact kathy.wang@aei.com.



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