IMMUNITY TO ELECTRO STATIC DISCHARGE

This technical note discusses the requirements for electro static discharge as outlined by the Eurepean Norm standard EN 61000-4-2 and provides some design techniques for meeting these requirements.

INTRODUCTION

Electrostatic discharge (ESD) can be defined as the transfer of electric charge between bodies of different electrostatic potential in proximity or through direct contact. The transfer of charge from one body to the other happens when two bodies have different charge particles (positive and negative).

TYPES OF ESD FAILURE

- Operational Failure (transient): Logic failures, reading errors or data loss caused by unwanted charging or discharging of internal capacitances.
- Catastrophic Failure (permanent): Device no longer functions due to metal melt, junction breakdown or oxide “punch-through”.
- Latent Failure (cumulative): Device still functions, but operating life is dramatically reduced by internal damages

ESD WAVEFORM CHARACTERISTIC

The graph indicates how much amplitude of the current with respect to time upon application of 4kV contact discharge.

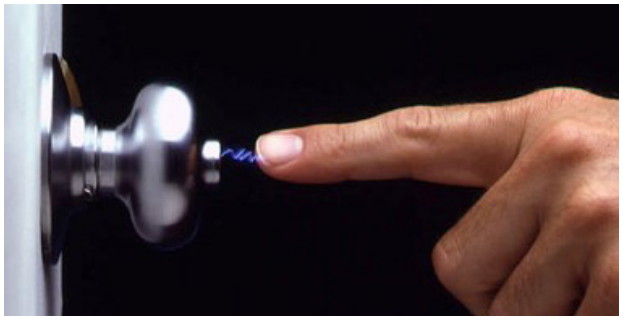

Figure 1: Paschen curves illustrate the dependency of breakdown voltage on distance between conductors and altitude

Table 1: Test Level, Test Voltage (KV)		
Level	**Contact Discharge**	**Air Discharge**
1	2	2
2	4	4
3	6	8
4	8	15
X	Special	Special

Table 1: 10 discharges per polarity on each selected points with discharge rate of 1 per second.

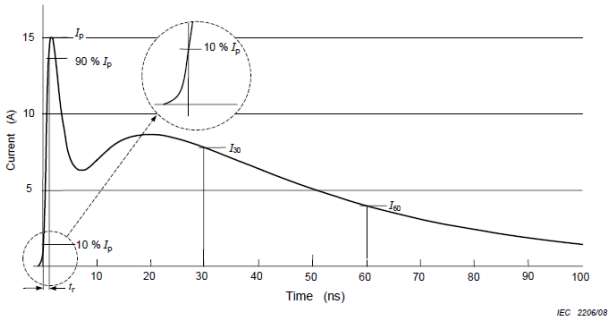

Figure 2: Contact discharge

APPLICABLE POINTS

Unless stated otherwise in the generic, product-related or product-family standards, the electrostatic discharges shall be applied only to those points and surfaces of the EUT which are accessible to persons during normal use.

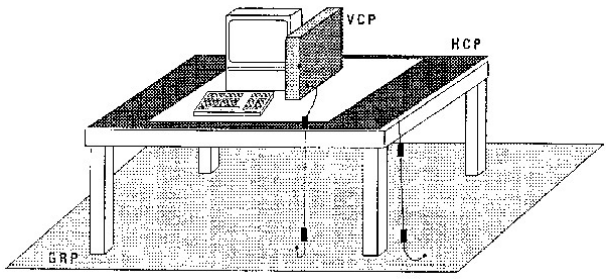

Figure 3: ESD test set up

ESD IMMUNITY DESIGN TECHNIQUES

1. Use of Transient Voltage Suppressors to clamp positive and voltage spikes on critical signals such as PGOK, ACOK typically signals that are exposed and going to the customer system.
2. Providing shortest path for the ESD current. This is obtained by layout and using y-caps that will direct the current out of the circuit through the chassis.
3. Insulation by using metal shielding, insulation through PCB separation or air separation.
4. Practically we can't put TVS on all critical PCB nets so the alternative way is to use limiting resistors in series with the critical pins of Analog/Digital IC's.

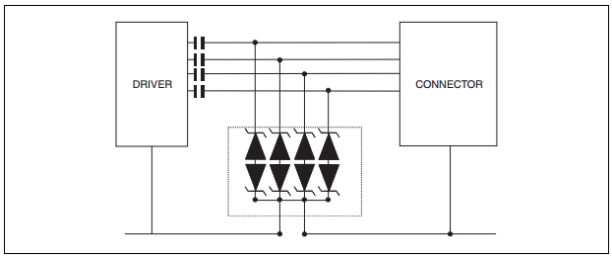

Figure 4: TVS typical application on critical nets

There are other ESD design improvements and ways to prevent ESD generation but the above items are mainly for PSU ESD immunity design.

REFERENCES

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6. EN 61000-4-3 – Cenelec
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8. EN 61000-4-5 – Cenelec
9. EN 61000-4-11 – Cenelec

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